Appendix

Report No.:	BCTC2504902986-2E
Applicant:	Shenzhen Huafurui Technology Co., Ltd.
Product Name:	Smartphone
Test Model:	P90
Tested Date:	2025-04-07 to 2025-06-11

Shenzhen BCTC Testing Co., Ltd.

C2-EPR Compliance Test Report

Test Summary - Overall

Total	Selected	PASS	FAIL	PASS Rate(%)	INCOMPLETE	NA	WARNING	NOT_SELECTED	ABORTED	NOT_EXECUTED
60	60	18	1	94%	0	41	0	0	0	0

Test Summary - All MOI

MOI Name	Total	PASS	FAIL	PASS Rate(%)	INCOMPLETE	NA	WARNING	NOT_SELECTED	ABORTED	NOT_EXECUTED
USB-C Functional Tests	60	18	1	94%	0	41	0	0	0	0

USB-C Functional Tests- Result Summary

Sl No	Test ID	Test Name	Test Result
1	TD.4.1.1	TD.4.1.1 Initial Voltage Test	PASS
2	TD.4.1.2	TD.4.1.2 Unpowered CC Voltage Test	NA
3	TD.4.2.1	TD.4.2.1 Source Connect Sink Test	NA
4	TD.4.2.2	TD.4.2.2 Source Connect SNKAS Test	NA
5	TD.4.2.3	TD.4.2.3 Source Connect DRP	NA
6	TD.4.2.4	TD.4.2.4 Source Connect Try SRC DRP	NA
7	TD.4.2.5	TD.4.2.5 Source Connect Try SNK DRP	NA
8	TD.4.2.6	TD.4.2.6 Source Connect Audio Accessory	NA
9	TD.4.2.7	TD.4.2.7 Source Connect Debug Accessory	NA
10	TD.4.2.8	TD.4.2.8 Source Connect Vconn Accessory	NA
11	TD.4.3.1	TD.4.3.1 Sink Connect Source Test	NA
12	TD.4.3.2	TD.4.3.2 Sink Connect DRP Test	NA
13	TD.4.3.3	TD.4.3.3 Sink Connect Try SRC DRP Test	NA
14	TD.4.3.4	TD.4.3.4 Sink Connect Try SNK DRP Test	NA
15	TD.4.3.5	TD.4.3.5 Sink.Connect.SNKAS.Test	NA
16	TD.4.3.6	TD.4.3.6 Sink.Connect.Accessories.Test	NA
17	TD.4.4.1	TD.4.4.1 SNKAS Connect Source Test	NA
18	TD.4.4.2	TD.4.4.2 SNKAS Connect DRP Test	NA
19	TD.4.4.3	TD.4.4.3 SNKAS Connect Try SRC DRP Test	NA
20	TD.4.4.4	TD.4.4.4 SNKAS Connect Try SNK DRP Test	NA
21	TD.4.4.5	TD.4.4.5 SNKAS Connect SNKAS Test	NA
22	TD.4.4.6	TD.4.4.6 SNKAS Connect Audio Acc	NA
23	TD.4.4.7	TD.4.4.7 SNKAS Connect Debug Accessory	NA
24	TD.4.4.8	TD.4.4.8 SNKAS Connect PoweredAcc	NA
25	TD.4.5.1	TD.4.5.1 DRP Connect Sink Test	NA
26	TD.4.5.2	TD.4.5.2 DRP Connect SNKAS Test	NA
27	TD.4.5.3	TD.4.5.3 DRP Connect Source Test	NA
28	TD.4.5.4	TD.4.5.4 DRP Connect DRP Test	NA
29	TD.4.5.5	TD.4.5.5 DRP Connect Try SRC DRP Test	NA
30	TD.4.5.6	TD.4.5.6 DRP Connect Try SNK DRP Test	NA

31	TD.4.6.1	TD.4.6.1 Try SRC DRP Connect Source Test	NA
32	TD.4.6.2	TD.4.6.2 Try SRC DRP Connect DRP Test	NA
33	TD.4.6.3	TD.4.6.3 Try SRC DRP Connect Try SRC DRP Test	NA
34	TD.4.6.4	TD.4.6.4 Try SRC DRP Connect Try SNK DRP Test	NA
35	TD.4.6.5	TD.4.6.5 Try SRC DRP Connect Sink Test	NA
36	TD.4.6.6	TD.4.6.6 Try SRC DRP Connect SNKAS Test	NA
37	TD.4.7.1	TD.4.7.1 Try SNK DRP Connect Source Test	PASS
38	TD.4.7.2	TD.4.7.2 Try SNK DRP Connect DRP Test	PASS
39	TD.4.7.3	TD.4.7.3 Try SNK DRP Connect Try SRC DRP Test	PASS
40	TD.4.7.4	TD.4.7.4 Try SNK DRP Connect Try SNK DRP Test	PASS
41	TD.4.7.5	TD.4.7.5 Try SNK DRP Connect Sink Test	PASS
42	TD.4.7.6	TD.4.7.6 Try SNK DRP Connect SNKAS Test	PASS
43	TD.4.8.1	TD.4.8.1 DRP Connect Audio Acc Test	PASS
44	TD.4.8.2	TD.4.8.2 DRP Connect Debug Acc Test	PASS
45	TD.4.8.3	TD.4.8.3 DRP Connect Vconn Accessory Test	PASS
46	TD.4.9.1	TD.4.9.1 Source Suspend Test	NA
47	TD.4.9.2	TD.4.9.2 USB Type C Current Advertisement Test	PASS
48	TD.4.9.3	TD.4.9.3 Source PR Swap Test	PASS
49	TD.4.9.4	TD.4.9.4 Source Vconn Swap Test	NA
50	TD.4.9.5	TD.4.9.5 Source Alternate Mode Test	NA
51	TD.4.10.1	TD.4.10.1 Sink Power Sub States Test	PASS
52	TD.4.10.2	TD.4.10.2 Sink Power Precedence Test	PASS
53	TD.4.10.3	TD.4.10.3 Sink Suspend Test	PASS
54	TD.4.10.4	TD.4.10.4 Sink PR Swap Test	PASS
55	TD.4.10.5	TD.4.10.5 Sink.VCONN Swap Test	NA
56	TD.4.10.6	TD.4.10.6 Sink Alternate Mode Test	PASS
57	TD.4.11.1	TD.4.11.1 DR Swap Test	PASS
58	TD.4.11.2	TD.4.11.2 Sink Dead Battery Test	PASS
59	TD.4.12.2	TD.4.12.2 Hub Port Types Test	NA
60	TD.4.13.5	TD.4.13.5 Cable EnterUSB and Data Reset Test	NA

USB-C Functional Tests - Detailed Test Result

Test Status	Test Description
PASS	**1. TD.4.1.1 Initial Voltage Test** (Click to View Protocol Trace)
PASS	DUT connection status: FSM_State_Disabled -> FSM_State_Unattached_SRC:
PASS	Step-4A: FSM_State_Disabled -> FSM_State_Unattached_SRC:
PASS	Step-4C: PUT's Vbus validation: Validation time range : 9.714sec to 10.447sec Expected voltage in PORTA_VBUS_VOLTAGE: Min = 0V and Max = 0.8V .Obtained voltage = 0.001V
PASS	Step-4D(1) : CVS transition to disabled:
PASS	Step-4D(ii): Ra_Asserted:
PASS	Step-4D(iv) PUT's Vbus validation: Validation time range : 11.255sec to 11.947sec Expected voltage in PORTA_VBUS_VOLTAGE: Min = 0V and Max = 0.8V .Obtained voltage = 0.001V
PASS	Step-4D(v) PUT's Vconn validation: Validation time range : 11.205sec to 11.947sec

Expected voltage in PORTA_CC2_VOLTAGE: Min = 0V and Max = 3V .Obtained voltage = 0.039V

PASS Step-7: Rp_Asserted - Vbus_CC_53k_Resistance_Applied:

Min= 740ms - Max = 760ms. Obtained time difference is 750.997ms

PASS Step-8: DRP shall not source Vbus:

Validation time range : 12.148sec to 12.449sec

Expected voltage in PORTA_VBUS_VOLTAGE: Min = 0V and Max = 0.8V .Obtained voltage = 0.001V

PASS Step-9: Rp_Asserted - Vbus_CC_53k_Resistance_Removed:

NA 2. TD.4.1.2 Unpowered CC Voltage Test (Click to View Protocol Trace)

PORT_BATTERY_POWERED is set to YES

NA 3. TD.4.2.1 Source Connect Sink Test (Click to View Protocol Trace)

Type_C_State_Machine Expected state: SRC. Obtained state: DRP

NA 4. TD.4.2.2 Source Connect SNKAS Test (Click to View Protocol Trace)

Type_C_State_Machine is not Source

NA 5. TD.4.2.3 Source Connect DRP (Click to View Protocol Trace)

Type_C_State_Machine is not Source

NA 6. TD.4.2.4 Source Connect Try SRC DRP (Click to View Protocol Trace)

Type_C_State_Machine is not Source

NA 7. TD.4.2.5 Source Connect Try SNK DRP (Click to View Protocol Trace)

Type_C_State_Machine is not Source

NA 8. TD.4.2.6 Source Connect Audio Accessory (Click to View Protocol Trace)

Type_C_State_Machine is not Source

NA 9. TD.4.2.7 Source Connect Debug Accessory (Click to View Protocol Trace)

Type_C_State_Machine is not Source

NA 10. TD.4.2.8 Source Connect Vconn Accessory (Click to View Protocol Trace)

Type_C_State_Machine is not Source

TYPE_C_SOURCES_VCONN is not set to YES

NA 11. TD.4.3.1 Sink Connect Source Test (Click to View Protocol Trace)

VIF field TYPE_C_SUPPORTS_AUDIO_ACCESSORY is not set to NO

Type_C_State_Machine is not set to sink

NA 12. TD.4.3.2 Sink Connect DRP Test (Click to View Protocol Trace)

Type_C_State_Machine is not set to sink

NA 13. TD.4.3.3 Sink Connect Try SRC DRP Test (Click to View Protocol Trace)

Type_C_State_Machine is not set to sink

NA 14. TD.4.3.4 Sink Connect Try SNK DRP Test (Click to View Protocol Trace)

Type_C_State_Machine is not set to sink

NA 15. TD.4.3.5 Sink.Connect.SNKAS.Test (Click to View Protocol Trace)

Type_C_State_Machine is not set to sink

NA 16. TD.4.3.6 Sink.Connect.Accessories.Test (Click to View Protocol

Trace)

Type_C_State_Machine is not set to SNK

NA 17. TD.4.4.1 SNKAS Connect Source Test (Click to View Protocol Trace)

Type_C_State machine is not set to SNK
TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES

NA 18. TD.4.4.2 SNKAS Connect DRP Test (Click to View Protocol Trace)

Type_C_State machine is not set to SNK
TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES

NA 19. TD.4.4.3 SNKAS Connect Try SRC DRP Test (Click to View Protocol Trace)

Type_C_State machine is not set to SNK
TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES

NA 20. TD.4.4.4 SNKAS Connect Try SNK DRP Test (Click to View Protocol Trace)

Type_C_State machine is not set to SNK
TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES

NA 21. TD.4.4.5 SNKAS Connect SNKAS Test (Click to View Protocol Trace)

Type_C_State machine is not set to SNK
TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES

NA 22. TD.4.4.6 SNKAS Connect Audio Acc (Click to View Protocol Trace)

Type_C_State machine is not set to SNK
TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES

NA 23. TD.4.4.7 SNKAS Connect Debug Accessory (Click to View Protocol Trace)

Type_C_State machine is not set to SNK
TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES

NA 24. TD.4.4.8 SNKAS Connect PoweredAcc (Click to View Protocol Trace)

Type_C_State machine is not set to SNK
TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES

NA 25. TD.4.5.1 DRP Connect Sink Test (Click to View Protocol Trace)

TYPE_C_IMPLEMENTS_TRY_SNK is not set to NO

NA 26. TD.4.5.2 DRP Connect SNKAS Test (Click to View Protocol Trace)

TYPE_C_IMPLEMENTS_TRY_SNK is not set to NO

NA 27. TD.4.5.3 DRP Connect Source Test (Click to View Protocol Trace)

TYPE_C_IMPLEMENTS_TRY_SNK is not set to NO

NA 28. TD.4.5.4 DRP Connect DRP Test (Click to View Protocol Trace)

TYPE_C_IMPLEMENTS_TRY_SNK is not set to NO

NA 29. TD.4.5.5 DRP Connect Try SRC DRP Test (Click to View Protocol Trace)

TYPE_C_IMPLEMENTS_TRY_SNK is not set to NO

NA 30. TD.4.5.6 DRP Connect Try SNK DRP Test (Click to View Protocol Trace)

TYPE_C_IMPLEMENTS_TRY_SNK is not set to NO

NA 31. TD.4.6.1 Try SRC DRP Connect Source Test (Click to View Protocol Trace)

TYPE_C_IMPLEMENTS_TRY_SRC is not set to YES

NA 32. TD.4.6.2 Try SRC DRP Connect DRP Test (Click to View Protocol Trace)

TYPE_C_IMPLEMENTS_TRY_SNK is not set to YES

NA 33. TD.4.6.3 Try SRC DRP Connect Try SRC DRP Test (Click to View Protocol Trace)

TYPE_C_IMPLEMENTS_TRY_SRC is not set to YES

NA 34. TD.4.6.4 Try SRC DRP Connect Try SNK DRP Test (Click to View Protocol Trace)

TYPE_C_IMPLEMENTS_TRY_SRC is not set to YES

NA 35. TD.4.6.5 Try SRC DRP Connect Sink Test (Click to View Protocol Trace)

TYPE_C_IMPLEMENTS_TRY_SRC is not set to YES

NA 36. TD.4.6.6 Try SRC DRP Connect SNKAS Test (Click to View Protocol Trace)

TYPE_C_IMPLEMENTS_TRY_SRC is not set to YES

PASS 37. TD.4.7.1 Try SNK DRP Connect Source Test (Click to View Protocol Trace)

PASS Step-1: FSM_State_Disabled -> FSM_State_Unattached_SRC:

PASS Step-3: Ra_Asserted:

Min= 4ms - Max = 8ms. Obtained time difference is 4.789ms

PASS Step-4A: FSM_State_Unattached_SRC -> FSM_State_AttachWait_SRC:

Min= 0ms - Max = 70ms. Obtained time difference is 16.899ms

PASS Step-4C: Rd asserted for tCCDebounce:

Validation time range : 3.618sec to 3.716sec

Expected voltage in PORTA_CC1_VOLTAGE: Min = 0.25V and Max = 2.45V .Obtained voltage = 1.043V

PASS Step-5: FSM_State_AttachWait_SRC -> FSM_State_Attached_SRC:

PASS Step - 6B : Validate PD contract:

PASS Step - 7 and 8 : Discover ID validation:

PASS Step-9: FSM_State_Attached_SRC -> FSM_State_Disabled:

PASS Step-10: Rd_Detected_Disabled:

PASS 38. TD.4.7.2 Try SNK DRP Connect DRP Test (Click to View Protocol Trace)

PASS tDRP and dc.SRC.DRP Timing condition 1:

PASS Step - 2: Ra_Asserted:

PASS Step - 3: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step - 3Bii: FSM_State_Unattached_SRC -> FSM_State_AttachWait_SRC:

PASS Step - 3Bii: FSM_State_AttachWait_SRC -> FSM_State_Attached_SRC:

PASS Step-4C : PUT's transition to Attached state:

PASS Step - 6 and 7 : VDM Validation:

PASS Step - 8: CVS programs Vbus source to meet 3.7V - VBUS_TST_PT_1:

Validation Range : 6.908sec to 6.918sec

Expected voltage : Min = 3.5V and Max = 3.8V . Obtained voltage = 3.701V

PASS : Regression Sequence:

PASS Step-9 : PUT remains in Attached.SNK:

PASS Step - 10: CVS removes Rps - VBUS_TST_PT_2:

PASS Step - 12: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step - 13 : PUT transitions to AttachWait.SRC within tDRP:

PASS Step-15 : PUT remains in Attachwait.SRC for 500ms:

Start time: 7.12S , Stop time: 7.615S

Expected CC line voltage range 0.25V - 2.45V , Obtained value -, Avg: 0.497V , Min: 0.496V and Max: 0.498V

PASS Step - 16: CVS removes Vbus source - VBUS_TST_PT_4:

PASS Step - 17: Rd_Detected:

PASS Step-18 : CVS transition to disabled state:

PASS tDRP and dc.SRC.DRP Timing condition 2:

PASS Step - 2: Ra_Asserted:

PASS Step - 3: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step - 3Bii: FSM_State_Unattached_SRC -> FSM_State_AttachWait_SRC:

PASS Step - 3Bii: FSM_State_AttachWait_SRC -> FSM_State_Attached_SRC:

PASS Step-4C : PUT's transition to Attached state:

PASS Step - 6 and 7 : VDM Validation:

PASS Step - 8: CVS programs Vbus source to meet 3.7V - VBUS_TST_PT_1:

Validation Range : 16.181sec to 16.191sec

Expected voltage : Min = 3.5V and Max = 3.8V . Obtained voltage = 3.701V

PASS : Regression Sequence:

PASS Step-9 : PUT remains in Attached.SNK:

PASS Step - 10: CVS removes Rps - VBUS_TST_PT_2:

PASS Step - 12: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step - 13 : PUT transitions to AttachWait.SRC within tDRP:

PASS Step-15 : PUT remains in Attachwait.SRC for 500ms:

Start time: 16.393S , Stop time: 16.888S

Expected CC line voltage range 0.25V - 2.45V , Obtained value -, Avg: 0.497V , Min: 0.496V and Max: 0.498V

PASS Step - 16: CVS removes Vbus source - VBUS_TST_PT_4:

PASS Step - 17: Rd_Detected:

PASS Step-18 : CVS transition to disabled state:

PASS tDRP and dc.SRC.DRP Timing condition 3:

PASS Step - 2: Ra_Asserted:

PASS Step - 3: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step - 3Bii: FSM_State_Unattached_SRC -> FSM_State_AttachWait_SRC:

PASS Step - 3Bii: FSM_State_AttachWait_SRC -> FSM_State_Attached_SRC:

PASS Step-4C : PUT's transition to Attached state:

PASS Step - 6 and 7 : VDM Validation:

PASS Step - 8: CVS programs Vbus source to meet 3.7V - VBUS_TST_PT_1:

Validation Range : 25.479sec to 25.489sec

Expected voltage : Min = 3.5V and Max = 3.8V . Obtained voltage = 3.701V

PASS : Regression Sequence:

PASS Step-9 : PUT remains in Attached.SNK:

PASS Step - 10: CVS removes Rps - VBUS_TST_PT_2:

PASS Step - 12: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step - 13 : PUT transitions to AttachWait.SRC within tDRP:

PASS Step-15 : PUT remains in Attachwait.SRC for 500ms:

Start time: 25.691S , Stop time: 26.186S

Expected CC line voltage range 0.25V - 2.45V , Obtained value -, Avg: 0.497V , Min: 0.496V and Max: 0.498V

PASS Step - 16: CVS removes Vbus source - VBUS_TST_PT_4:

PASS Step - 17: Rd_Detected:

PASS Step-18 : CVS transition to disabled state:

PASS tDRP and dc.SRC.DRP Timing condition 4:

PASS Step - 2: Ra_Asserted:

PASS Step - 3: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step - 3Bii: FSM_State_Unattached_SRC -> FSM_State_AttachWait_SRC:

PASS Step - 3Bii: FSM_State_AttachWait_SRC -> FSM_State_Attached_SRC:

PASS Step-4C : PUT's transition to Attached state:

PASS Step - 6 and 7 : VDM Validation:

PASS Step - 8: CVS programs Vbus source to meet 3.7V - VBUS_TST_PT_1:

Validation Range : 34.727sec to 34.737sec

Expected voltage : Min = 3.5V and Max = 3.8V . Obtained voltage = 3.7V

PASS : Regression Sequence:

PASS Step-9 : PUT remains in Attached.SNK:

PASS Step - 10: CVS removes Rps - VBUS_TST_PT_2:

PASS Step - 12: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step - 13 : PUT transitions to AttachWait.SRC within tDRP:

PASS Step-15 : PUT remains in Attachwait.SRC for 500ms:

Start time: 34.939S , Stop time: 35.434S

Expected CC line voltage range 0.25V - 2.45V , Obtained value -, Avg: 0.497V , Min: 0.496V and Max: 0.498V

PASS Step - 16: CVS removes Vbus source - VBUS_TST_PT_4:

PASS Step - 17: Rd_Detected:

PASS Step-18 : CVS transition to disabled state:

PASS tDRP and dc.SRC.DRP Timing condition 5:

PASS Step - 2: Ra_Asserted:

PASS Step - 3: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step - 3Bii: FSM_State_Unattached_SRC -> FSM_State_AttachWait_SRC:

PASS Step - 3Bii: FSM_State_AttachWait_SRC -> FSM_State_Attached_SRC:

PASS Step-4C : PUT's transition to Attached state:

PASS Step - 6 and 7 : VDM Validation:

PASS Step - 8: CVS programs Vbus source to meet 3.7V - VBUS_TST_PT_1:

Validation Range : 44sec to 44.01sec

Expected voltage : Min = 3.5V and Max = 3.8V . Obtained voltage = 3.701V

PASS : Regression Sequence:

PASS Step-9 : PUT remains in Attached.SNK:

PASS Step - 10: CVS removes Rps - VBUS_TST_PT_2:

PASS Step - 12: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step - 13 : PUT transitions to AttachWait.SRC within tDRP:

PASS Step-15 : PUT remains in Attachwait.SRC for 500ms:

Start time: 44.213S , Stop time: 44.708S

Expected CC line voltage range 0.25V - 2.45V , Obtained value -, Avg: 0.497V , Min: 0.496V and Max: 0.498V

PASS Step - 16: CVS removes Vbus source - VBUS_TST_PT_4:

PASS Step - 17: Rd_Detected:

PASS Step-18 : CVS transition to disabled state:

PASS tDRP and dc.SRC.DRP Timing condition 6:

PASS Step - 2: Ra_Asserted:

PASS Step - 3: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step - 3Bii: FSM_State_Unattached_SRC -> FSM_State_AttachWait_SRC:

PASS Step - 3Bii: FSM_State_AttachWait_SRC -> FSM_State_Attached_SRC:

PASS Step-4C : PUT's transition to Attached state:

PASS Step - 6 and 7 : VDM Validation:

PASS Step - 8: CVS programs Vbus source to meet 3.7V - VBUS_TST_PT_1:

Validation Range : 53.303sec to 53.313sec

Expected voltage : Min = 3.5V and Max = 3.8V . Obtained voltage = 3.7V

PASS : Regression Sequence:

PASS Step-9 : PUT remains in Attached.SNK:

PASS Step - 10: CVS removes Rps - VBUS_TST_PT_2:

PASS Step - 12: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step - 13 : PUT transitions to AttachWait.SRC within tDRP:

PASS Step-15 : PUT remains in Attachwait.SRC for 500ms:

Start time: 53.516S , Stop time: 54.011S

Expected CC line voltage range 0.25V - 2.45V , Obtained value -, Avg: 0.497V , Min: 0.496V and Max: 0.498V

PASS Step - 16: CVS removes Vbus source - VBUS_TST_PT_4:

PASS Step - 17: Rd_Detected:

PASS Step-18 : CVS transition to disabled state:

PASS tDRP and dc.SRC.DRP Timing condition 7:

PASS Step - 2: Ra_Asserted:

PASS Step - 3: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step - 3Bii: FSM_State_Unattached_SRC -> FSM_State_AttachWait_SRC:

PASS Step - 3Bii: FSM_State_AttachWait_SRC -> FSM_State_Attached_SRC:

PASS Step-4C : PUT's transition to Attached state:

PASS Step - 6 and 7 : VDM Validation:

PASS Step - 8: CVS programs Vbus source to meet 3.7V - VBUS_TST_PT_1:

Validation Range : 62.552sec to 62.562sec

Expected voltage : Min = 3.5V and Max = 3.8V . Obtained voltage = 3.7V

PASS : Regression Sequence:

PASS Step-9 : PUT remains in Attached.SNK:

PASS Step - 10: CVS removes Rps - VBUS_TST_PT_2:

PASS Step - 12: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step - 13 : PUT transitions to AttachWait.SRC within tDRP:

PASS Step-15 : PUT remains in Attachwait.SRC for 500ms:

Start time: 62.763S , Stop time: 63.258S

Expected CC line voltage range 0.25V - 2.45V , Obtained value -, Avg: 0.497V , Min: 0.496V and Max: 0.498V

PASS Step - 16: CVS removes Vbus source - VBUS_TST_PT_4:

PASS Step - 17: Rd_Detected:

PASS Step-18 : CVS transition to disabled state:

PASS tDRP and dc.SRC.DRP Timing condition 8:

PASS Step - 2: Ra_Asserted:

PASS Step - 3: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step - 3Bii: FSM_State_Unattached_SRC -> FSM_State_AttachWait_SRC:

PASS Step - 3Bii: FSM_State_AttachWait_SRC -> FSM_State_Attached_SRC:

PASS Step-4C : PUT's transition to Attached state:

PASS Step - 6 and 7 : VDM Validation:

PASS Step - 8: CVS programs Vbus source to meet 3.7V - VBUS_TST_PT_1:

Validation Range : 71.825sec to 71.835sec

Expected voltage : Min = 3.5V and Max = 3.8V . Obtained voltage = 3.701V

PASS : Regression Sequence:

PASS Step-9 : PUT remains in Attached.SNK:

PASS Step - 10: CVS removes Rps - VBUS_TST_PT_2:

PASS Step - 12: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step - 13 : PUT transitions to AttachWait.SRC within tDRP:

PASS Step-15 : PUT remains in Attachwait.SRC for 500ms:

Start time: 72.037S , Stop time: 72.532S

Expected CC line voltage range 0.25V - 2.45V , Obtained value -, Avg: 0.497V , Min: 0.496V and Max: 0.498V

PASS Step - 16: CVS removes Vbus source - VBUS_TST_PT_4:

PASS Step - 17: Rd_Detected:

PASS Step-18 : CVS transition to disabled state:

PASS tDRP and dc.SRC.DRP Timing condition 9:

PASS Step - 2: Ra_Asserted:

PASS Step - 3: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step - 3Bii: FSM_State_Unattached_SRC -> FSM_State_AttachWait_SRC:

PASS Step - 3Bii: FSM_State_AttachWait_SRC -> FSM_State_Attached_SRC:

PASS Step-4C : PUT's transition to Attached state:

PASS Step - 6 and 7 : VDM Validation:

PASS Step - 8: CVS programs Vbus source to meet 3.7V - VBUS_TST_PT_1:

Validation Range : 81.123sec to 81.133sec

Expected voltage : Min = 3.5V and Max = 3.8V . Obtained voltage = 3.699V

PASS : Regression Sequence:

PASS Step-9 : PUT remains in Attached.SNK:

PASS Step - 10: CVS removes Rps - VBUS_TST_PT_2:

PASS Step - 12: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step - 13 : PUT transitions to AttachWait.SRC within tDRP:

PASS Step-15 : PUT remains in Attachwait.SRC for 500ms:

Start time: 81.334S , Stop time: 81.829S

Expected CC line voltage range 0.25V - 2.45V , Obtained value -, Avg: 0.497V , Min: 0.496V and Max: 0.498V

PASS Step - 16: CVS removes Vbus source - VBUS_TST_PT_4:

PASS Step - 17: Rd_Detected:

PASS Step-18 : CVS transition to disabled state:

PASS **39. TD.4.7.3 Try SNK DRP Connect Try SRC DRP Test** (Click to View Protocol Trace)

PASS Step-1 : FSM transition from disabled to unattahced.SNK:

PASS Step-4 : FSM transition from unattahced.SNK to AttachWait.SNK:

PASS Step-3A : PUT presents Rp within tDRP – dcSRC.DRP x tDRP:

Min= 0ms - Max = 75ms. Obtained time difference is 11.992ms

Step-6 : FSM transition from AttachWait.SNK to Unattached.SRC:

PASS

PASS Step-5 : PUT keeps Rp attached in for tCCDebounce:

Min= 100ms - Max = 201ms. Obtained time difference is 158.725ms

PASS Step-6 : PUT transitions to Try.SNK within tCCDebounce max + tDRPTransition:

Min= 0ms - Max = 201ms. Obtained time difference is 158.725ms

PASS Step-7 : FSM transition from unattached.SRC to attachWait.SRC:

PASS Step-8 : FSM transition from attachWait.SRC to attached.SRC:

PASS Step-9B : Validate PD contract:

PASS Step-10 : FSM transition from attached.SRC to disabled:

PASS Step-11 : PUT's transition to Unattached.SNK:

Min= 0ms - Max = 650ms. Obtained time difference is 25.55ms

PASS **40. TD.4.7.4 Try SNK DRP Connect Try SNK DRP Test** (Click to View Protocol Trace)

PASS Step-1: FSM transition from disabled to unattahced.SNK:

PASS Step-3,4: FSM transition from unattahced.SNK to AttachWait.SNK:

Min= 0ms - Max = 75ms. Obtained time difference is 36.833ms

PASS Step-5: PUT should provide Rd for tCCDebounce:

Validation time range : 4.235sec to 4.335sec

Expected voltage in PORTA_CC1_VOLTAGE: Min = 0.25V and Max = 2.45V .Obtained voltage = 0.497V

PASS Step-6: FSM transition from AttachWait.SNK to AttachWait.SRC:

Min= 200ms - Max = 205ms. Obtained time difference is 200.002ms

PASS Step-7: FSM transition from AttachWait.SRC to Try.SNK:

PASS Step-9: Transition from Try.SNK to Attached.SNK:

Min= 10ms - Max = 445ms. Obtained time difference is 168.643ms

PASS Step-9B: PDC validation:

PASS Step-10: FSM transition from attached.SNK to disabled:

PASS Step-11: PUT transitions to Unattached.SNK before tVBUSOFF expires:

Min= 0ms - Max = 650ms. Obtained time difference is 3.493ms

PASS **41. TD.4.7.5 Try SNK DRP Connect Sink Test** (Click to View Protocol Trace)

PASS USB PD 2.0 5A Active cable:

PASS Step-1 : PUT does not source Vconn:

PASS Vconn validation:

Validation time range : 3.611sec to 9.419sec

Expected voltage in PORTA_CC2_VOLTAGE: Min = 0V and Max = 3V .Obtained voltage = 0.361V

PASS Step-3: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step-5,6: FSM_State_Unattached_SNK -> FSM_State_AttachWait_SNK:

Min= 0ms - Max = 70ms. Obtained time difference is 8.615ms

PASS Step - 7A: PUT should assert Rp for tCCDebounce:

Validation time range : 3.624sec to 3.724sec

Expected voltage in PORTA_CC1_VOLTAGE: Min = 0.25V and Max = 2.45V .Obtained voltage = 0.497V

PASS Step-7B: FSM_State_AttachWait_SNK -> FSM_State_Unattached_SNK:

PASS Step-7C: FSM_State_Unattached_SNK -> FSM_State_AttachWait_SNK:

PASS Step - 8A: PUT source vbus within tVbusON:

Validation time range : 4.369sec to 4.373sec

Expected voltage in PORTA_VBUS_VOLTAGE: Min = 4.75V and Max = 5.5V .Obtained voltage = 5.086V

PASS Step - 8D(i)(2) : Validate PD contract:

PASS Step-8: FSM_State_AttachWait_SNK -> FSM_State_Attached_SNK:

PASS Step-9: FSM_State_Attached_SNK -> FSM_State_Disabled:

PASS Step-10: Rd_Detected_Disabled:

Min= 0ms - Max = 650ms. Obtained time difference is 1.877ms

PASS USB PD 3.0 5A Active cable:

PASS Step-1 : PUT does not source Vconn:

PASS Vconn validation:

Validation time range : 9.419sec to 15.227sec

Expected voltage in PORTA_CC2_VOLTAGE: Min = 0V and Max = 3V .Obtained voltage = 0.361V

PASS Step-3: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step-5,6: FSM_State_Unattached_SNK -> FSM_State_AttachWait_SNK:

Min= 0ms - Max = 70ms. Obtained time difference is 39.931ms

PASS Step - 7A: PUT should assert Rp for tCCDebounce:

Validation time range : 9.465sec to 9.563sec

Expected voltage in PORTA_CC1_VOLTAGE: Min = 0.25V and Max = 2.45V .Obtained voltage = 0.497V

PASS Step-7B: FSM_State_AttachWait_SNK -> FSM_State_Unattached_SNK:

PASS Step-7C: FSM_State_Unattached_SNK -> FSM_State_AttachWait_SNK:

PASS Step - 8A: PUT source vbus within tVbusON:

Validation time range : 10.211sec to 10.214sec

Expected voltage in PORTA_VBUS_VOLTAGE: Min = 4.75V and Max = 5.5V .Obtained voltage = 5.085V

PASS Step - 8D(i)(2) : Validate PD contract:

PASS Step-8: FSM_State_AttachWait_SNK -> FSM_State_Attached_SNK:

PASS Step-9: FSM_State_Attached_SNK -> FSM_State_Disabled:

PASS Step-10: Rd_Detected_Disabled:

Min= 0ms - Max = 650ms. Obtained time difference is 3.663ms

PASS USB4 re-driver cable:

PASS Step-1 : PUT does not source Vconn:

PASS Vconn validation:

Validation time range : 15.227sec to 18.941sec

Expected voltage in PORTA_CC2_VOLTAGE: Min = 0V and Max = 3V .Obtained voltage = 0.361V

PASS Step-3: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step-5,6: FSM_State_Unattached_SNK -> FSM_State_AttachWait_SNK:

Min= 0ms - Max = 70ms. Obtained time difference is 44.993ms

PASS Step - 7A: PUT should assert Rp for tCCDebounce:

Validation time range : 15.278sec to 15.376sec

Expected voltage in PORTA_CC1_VOLTAGE: Min = 0.25V and Max = 2.45V .Obtained voltage = 0.497V

PASS Step-7B: FSM_State_AttachWait_SNK -> FSM_State_Unattached_SNK:

PASS Step-7C: FSM_State_Unattached_SNK -> FSM_State_AttachWait_SNK:

PASS Step - 8A: PUT source vbus within tVbusON:

Validation time range : 16.02sec to 16.022sec

Expected voltage in PORTA_VBUS_VOLTAGE: Min = 4.75V and Max = 5.5V .Obtained voltage = 5.087V

PASS Step - 8D(i)(2) : Validate PD contract:

PASS Step-8: FSM_State_AttachWait_SNK -> FSM_State_Attached_SNK:

PASS Step-9: FSM_State_Attached_SNK -> FSM_State_Disabled:

PASS Step-10: Rd_Detected_Disabled:

Min= 0ms - Max = 650ms. Obtained time difference is 4.137ms

PASS **42. TD.4.7.6 Try SNK DRP Connect SNKAS Test** (Click to View Protocol Trace)

PASS Step-1 : FSM transition from disabled to unattahced.SNK:

PASS Step-[2-4] : FSM transition from unattahced.SNK to AttachWait.SNK:

Min= 0ms - Max = 75ms. Obtained time difference is 35.961ms

PASS Step-5 : FSM transition from AttachWait.SNK to Unattached.SNK:

Min= 100ms - Max = 300ms. Obtained time difference is 158.725ms

PASS Step-7 : FSM transition from unattahced.SNK to Unattached.Accessory:

Min= 15ms - Max = 150ms. Obtained time difference is 49.974ms

PASS Step-7A : FSM transition from Unattached.Accessory to unattahced.SNK :

PASS Step-9 : PUT attaches Rp after CVS transitions to Unattached.SNK:

PASS Step-10 : FSM transition from unattahced.SNK to attachwait.SNK:

PASS Step-10 : FSM transition from attachwait.SNK to attached.SNK:

PASS Step-10B : PD contract validation:

PASS Step-11 : FSM transition from attached.SNK to disabled:

PASS Step-12 : PUT's transition to Unattached.SNK:

PASS Step-14 : Ra assertion in one cc:

PASS Step-1 : FSM transition from disabled to unattahced.SNK:

PASS Step-[2-4] : FSM transition from unattahced.SNK to AttachWait.SNK:

PASS Step-6 : FSM transition from AttachWait.SNK to Unattached.SNK:

PASS Step-15 : FSM transition to Powered.Accessory:

PASS Step-[16-17] : Vconn powered accessory validation:

PASS Step-18B : PUT's transition to TryWait.SRC:

PASS Step-9 : FSM transition from Try.SNK to attached.SNK:

Min= 10ms - Max = 295ms. Obtained time difference is 32.035ms

PASS Step-9 : Validate PD contract:

PASS Step-10 : FSM transition from attached.SNK to disabled:

PASS Step-11 : PUT's transition to Unattached.SNK:

PASS **43. TD.4.8.1 DRP Connect Audio Acc Test** (Click to View Protocol Trace)

PASS Step - 1: Ra_Asserted:

PASS Step - 3(ii): PUT should not source vbus:

Validation time range : 4.399sec to 7.582sec

Expected voltage in PORTA_VBUS_VOLTAGE: Min = 0V and Max = 0.8V .Obtained voltage = 0.001V

PASS Step - 3(ii): PUT should not source vconn:

Validation time range : 3.586sec to 7.582sec

Expected voltage in PORTA_CC2_VOLTAGE: Min = 0V and Max = 3V .Obtained voltage = 0.497V

PASS Step - 3(ii): PUT should not source vconn:

Validation time range : 3.583sec to 7.582sec

Expected current in PORTA_VBUS_CURRENT: Min = 0A and Max = 0.5A .Obtained current = 0.004A

PASS Step - 5: Ra_Removed:

PASS Step - 6: Rp_Detected_Disabled:

PASS **44. TD.4.8.2 DRP Connect Debug Acc Test** (Click to View Protocol

Trace)

PASS Step - 1: Rd_Asserted:

PASS Step - 3: PUT should source Vbus:

Validation time range : 3.835sec to 4.09sec

Expected voltage in PORTA_VBUS_VOLTAGE: Min = 4.75V and Max = 5.5V .Obtained voltage = 5.088V

PASS Step - 2: : PUT transitions to Unattached.SRC:

PASS Step - 5: FSM_State_Debug_Test_Sys_Snk -> FSM_State_Disabled:

PASS **45. TD.4.8.3 DRP Connect Vconn Accessory Test** (Click to View Protocol Trace)

PASS Step - 1: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step - 2: FSM_State_Unattached_SNK -> FSM_State_AttachWait_SNK:

Min= 0ms - Max = 70ms. Obtained time difference is 31.527ms

PASS Step - 3A(i) : PUT transitions to Try.SNK within tCCDebounce:

Start time : 3.635S

Should be less than 200ms. Obtained time 136.0343ms

PASS Step - 3A(ii): Attach:

Start time: 3.771S

Should be less than 170ms. Obtained time 127.8648ms

PASS Step - 4: FSM_State_AttachWait_SNK -> FSM_State_Attached_SNK:

PASS Step - 4A : PUT sources Vbus within tTryCCDebounce + tVbusON:

PASS Vbus validation:

Validation time range : 4.02sec to 4.194sec

Expected voltage in PORTA_VBUS_VOLTAGE: Min = 4.75V and Max = 5.5V .Obtained voltage = 5.085V

PASS Step - 4D(i) : Validate PD contract:

PASS Step - 5: FSM_State_Attached_SNK -> FSM_State_Disabled:

PASS Step - 6: Rd_Detected_Disabled:

PASS Step - 5A: PUT stops sourcing Vconn:

Validation time range : 67.612sec to 67.647sec

Expected voltage in PORTA_CC2_VOLTAGE: Min = 0V and Max = 3V .Obtained voltage = 0.007V

PASS Step - 5B: PUT stops sourcing Vbus:

Validation time range : 67.625sec to 68.262sec

Expected voltage in PORTA_VBUS_VOLTAGE: Min = 0V and Max = 0.8V .Obtained voltage = 0.002V

NA **46. TD.4.9.1 Source Suspend Test** (Click to View Protocol Trace)

DUT is not PUT_V

PASS **47. TD.4.9.2 USB Type C Current Advertisement Test** (Click to View Protocol Trace)

PASS Step - 1: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step - 2: FSM_State_Unattached_SNK -> FSM_State_AttachWait_SNK:

PASS Step - 3: FSM_State_AttachWait_SNK -> FSM_State_Attached_SNK:

NA Step - 5 : Rp validation based on BC_1_2 support:

PUT doesn't support BC 1.2

PASS Step - 6A: Ra_Asserted:

PASS Step - 6C : PUT's Rp range as per advertised PDO:

PASS Rp validation:

Validation time range : 4.152sec to 4.314sec

Expected voltage in PORTA_CC1_VOLTAGE: Min = 0.25V

and Max = 0.61V .Obtained voltage = 0.497V

PASS Step - 6D: FSM_State_Attached_SNK -> FSM_State_Disabled:

PASS Step - 6F: FSM_State_Disabled -> FSM_State_Unattached_SNK:

Min= 746ms - Max = 754ms. Obtained time difference is 751.828ms

PASS Step - 6G: FSM_State_Unattached_SNK -> FSM_State_AttachWait_SNK:

PASS Step - 6G: FSM_State_AttachWait_SNK -> FSM_State_Attached_SNK:

PASS Step - 6I(ii) : PUT should not advertise PDO with max current greater than 3A:

Source capabilities message at 6.908s

PASS Step - 6J(i) : Validate PD contract:

PASS Step - 6J(ii) : PUT's Rp range as per advertised PDO:

PASS Rp validation:

Validation time range : 6.368sec to 8.352sec

Expected voltage in PORTA_CC1_VOLTAGE: Min = 0.45V and Max = 2.45V .Obtained voltage = 1.317V

PASS : FSM_State_Attached_SNK -> FSM_State_Disabled:

PASS **48. TD.4.9.3 Source PR Swap Test** (Click to View Protocol Trace)

PASS Step - 1: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step - 2: Ra_Asserted:

PASS Step - 3: FSM_State_Unattached_SNK -> FSM_State_AttachWait_SNK:

PASS Step - 4: FSM_State_AttachWait_SNK -> FSM_State_Attached_SNK:

PASS Step - 6 : PR_Swap validation:

PASS Step - 8: FSM_State_Attached_SRC -> FSM_State_Disabled:

PASS DUT should maintain its data role:

NA **49. TD.4.9.4 Source Vconn Swap Test** (Click to View Protocol Trace)

PUT is not PUT_V

VIF field VCONN_SWAP_TO_OFF_SUPPORTED is not set to YES

NA **50. TD.4.9.5 Source Alternate Mode Test** (Click to View Protocol Trace)

VIF field TYPE_C_IS_ALT_MODE_CONTROLLER is not set to YES

FAIL **51. TD.4.10.1 Sink Power Sub States Test** (Click to View Protocol Trace)

PASS Step - 1: FSM_State_Disabled -> FSM_State_Unattached_SRC:

PASS Step - 2: FSM_State_Unattached_SRC -> FSM_State_AttachWait_SRC:

PASS Step - 3: FSM_State_AttachWait_SRC -> FSM_State_Attached_SRC:

PASS Step-4 : PUT shall not draw more than default USB power:

Time interval 3.856s - 3.91sExpected value in PORTA_VBUS_CURRENT: Min = 0A and Max = 0.1A . Obtained value is 0.005A

PASS Step - 7: Rp_Asserted - Rp_12k_1_5A_Asserted:

PASS Step-8 : PUT's vbus current validation:

PASS Step-8A - PUT draws no more than default USB power before min tPDDebounce:

Time interval 3.802s - 3.812sExpected value in PORTA_VBUS_CURRENT: Min = 0A and Max = 0.1A . Obtained value is 0.003A

PASS Step-8B - PUT draws no more than 1.5 amps after max tPDDebounce:

Time interval 3.822s - 4.822sExpected value in PORTA_VBUS_CURRENT: Min = 0A and Max = 1.5A . Obtained value is 0.236A

FAIL Step-10 : The PUT draws no more than default USB power after max tSinkAdj:

Time interval 10.652s - 11.652sExpected value in PORTA_VBUS_CURRENT: Min = 0A and Max = 0.1A . Obtained value is 0.45A

PASS Step - 9: Rp_Asserted - Rp_36k_900mA_Asserted:

PASS Step - 11: Rp_Asserted - Rp_4_7k_3A_Asserted:

FAIL Step-12 : PUT's vbus current validation:

Time interval 13.595s - 13.605sExpected value in PORTA_VBUS_CURRENT: Min = 0A and Max = 0.1A . Obtained value is 0.449A

Time interval 13.615s - 14.615sExpected value in PORTA_VBUS_CURRENT: Min = 0A and Max = 3A . Obtained value is 0.45A

PASS Step - 13: Rp_Asserted - Rp_12k_1_5A_Asserted:

PASS Step-14 : PUT draws no more than 1.5 amps after max tSinkAdj:

Time interval 16.658s - 17.658sExpected value in PORTA_VBUS_CURRENT: Min = 0A and Max = 1.5A . Obtained value is 0.45A

PASS Step - 15: Rp_Asserted - Rp_4_7k_3A_Asserted:

PASS Step-16 : PUT's Vbus current validation:

Time interval 19.601s - 19.611sExpected value in PORTA_VBUS_CURRENT: Min = 0A and Max = 1.5A . Obtained value is 0.45A

Time interval 19.621s - 20.621sExpected value in PORTA_VBUS_CURRENT: Min = 0A and Max = 3A . Obtained value is 0.449A

PASS Step - 17: Rp_Asserted - Rp_36k_900mA_Asserted:

FAIL Step-18 : PUT draws no more than default USB after max tSinkAdj:

Time interval 22.664s - 23.664sExpected value in PORTA_VBUS_CURRENT: Min = 0A and Max = 0.1A . Obtained value is 0.449A

PASS Step - 19: FSM_State_Attached_SRC -> FSM_State_Disabled:

PASS Step - 21: FSM_State_Disabled -> FSM_State_Unattached_SRC:

PASS Step - 22: FSM_State_Unattached_SRC -> FSM_State_AttachWait_SRC:

PASS Step - 22: FSM_State_AttachWait_SRC -> FSM_State_Attached_SRC:

PASS Step-23 : PUT's vbus current validation:

Time interval 26.075s - 26.085sExpected value in PORTA_VBUS_CURRENT: Min = 0A and Max = 0.1A . Obtained value is 0.004A

Time interval 26.095s - 27.095sExpected value in PORTA_VBUS_CURRENT: Min = 0A and Max = 1.5A . Obtained value is 0.26A

PASS Step - 26: FSM_State_Attached_SRC -> FSM_State_Disabled:

PASS Step - 28: FSM_State_Disabled -> FSM_State_Unattached_SRC:

PASS Step - 29: FSM_State_Unattached_SRC -> FSM_State_AttachWait_SRC:

PASS Step - 29: FSM_State_AttachWait_SRC -> FSM_State_Attached_SRC:

PASS Step-30 : PUT's vbus current validation:

Time interval 28.285s - 28.295sExpected value in PORTA_VBUS_CURRENT: Min = 0A and Max = 0.1A . Obtained value is 0.002A

Time interval 28.305s - 29.305sExpected value in PORTA_VBUS_CURRENT: Min = 0A and Max = 3A . Obtained value is 0.263A

PASS **52. TD.4.10.2 Sink Power Precedence Test** (Click to View Protocol Trace)

PASS Step - 1: FSM_State_Disabled -> FSM_State_Unattached_SRC:

PASS Step - 2: FSM_State_Unattached_SRC -> FSM_State_AttachWait_SRC:

PASS Step - 2: FSM_State_AttachWait_SRC -> FSM_State_Attached_SRC:

PASS Step - 4 : PUT sinks current within USB 2.0 power requirement:

PASS PUT's current measurement:

Validation time range : 3.86sec to 4.008sec

Expected current in PORTA_VBUS_CURRENT: Min = 0A and Max = 0.5A .Obtained current = 0.002A

PASS Step - 6: Rp_Asserted - Rp_4_7k_3A_Asserted:

PASS Step - 7 : PUT's vbus current validation:

Time interval 4.028s - 5.028sExpected value in PORTA_VBUS_CURRENT: Min = 0A and Max = 3A . Obtained value is 0.304A

PASS Step - 8: FSM_State_Attached_SRC -> FSM_State_Disabled:

PASS Step - 9: FSM_State_Disabled -> FSM_State_Unattached_SRC:

PASS Step - 10: FSM_State_Unattached_SRC -> FSM_State_AttachWait_SRC:

PASS Step - 10: FSM_State_AttachWait_SRC -> FSM_State_Attached_SRC:

PASS Step - 13: Rp_Asserted - Rp_4_7k_3A_Asserted:

PASS Step - 14 : PUT's vbus current validation:

Time interval 4.028s - 5.028sExpected value in PORTA_VBUS_CURRENT: Min = 0A and Max = 3A . Obtained value is 0.304A

PASS Step - 15A: Rp_Asserted - Rp_12k_1_5A_Asserted:

PASS Step - 15B(i) : Validate PD contract:

PASS Step - 15B(ii) : PUT's vbus current validation:

Time interval 4.067s - 5.067sExpected value in PORTA_VBUS_CURRENT: Min = 0A and Max = 1.5A . Obtained value is 0.322A

PASS Step - 15E: Rp_Asserted - Rp_4_7k_3A_Asserted:

PASS Step - 15D : Step - 15: PUT should not draw more than 1.5A:

Time interval 16.405s - 17.405sExpected value in PORTA_VBUS_CURRENT: Min = 0A and Max = 1.5A . Obtained value is 0.449A

PASS Step - 15G : CVS initiates hard reset:

PASS Step - 15H : CVS advertises vRd-USB on its Rp:

PASS Step - 15J : PUT sinks current based on device speed:

Time interval 19.624s - 20.624sExpected value in PORTA_VBUS_CURRENT: Min = 0A and Max = 0.1A . Obtained value is 0.099A

PASS **53. TD.4.10.3 Sink Suspend Test** (Click to View Protocol Trace)

PASS Step - 1: FSM_State_Disabled -> FSM_State_Unattached_SRC:

PASS Step - 2: FSM_State_Unattached_SRC -> FSM_State_AttachWait_SRC:

PASS Step - 2: FSM_State_AttachWait_SRC -> FSM_State_Attached_SRC:

PASS Step - 5: FSM_State_Attached_SRC -> FSM_State_Disabled:

PASS Step - 6: FSM_State_Disabled -> FSM_State_Unattached_SRC:

PASS Step - 9: FSM_State_Attached_SRC -> FSM_State_Disabled:

PASS Step - 10: FSM_State_Disabled -> FSM_State_Unattached_SRC:

PASS Step - 13: FSM_State_Attached_SRC -> FSM_State_Disabled:

PASS Step - 14: FSM_State_Disabled -> FSM_State_Unattached_SRC:

PASS **54. TD.4.10.4 Sink PR Swap Test** (Click to View Protocol Trace)

PASS Step - 1: FSM_State_Disabled -> FSM_State_Unattached_SRC:

PASS Step - 3: FSM_State_Unattached_SRC -> FSM_State_AttachWait_SRC:

PASS Step - 4: FSM_State_AttachWait_SRC -> FSM_State_Attached_SRC:

PASS Step - 6 : Validate PD contract:

PASS Step - 7 : PR_Swap validation:

PASS Step-9B : PUT_R does not source VCONN:

Expected voltage: 0V - 3V. Obtained voltage: 0.094V
Start time: 5.948S and stop time: 5.949S

PASS Step - 9C : DUT should maintain its data role:

PASS Step - 11: FSM_State_Attached_SNK -> FSM_State_Disabled:

PASS Step-12 : PUT transition to unattached within tDetach:

Min= 0ms - Max = 20ms. Obtained time difference is 3.371ms

PASS Step - 12B: Rd_Detected_Disabled:

PASS Step - 12C: PUT stops sourcing vbus within tVbusOFF:

Validation time range : 8.253sec to 8.352sec
Expected voltage in PORTA_VBUS_VOLTAGE: Min = 0V

and Max = 0.8V .Obtained voltage = 0.001V

NA 55. TD.4.10.5 Sink.VCONN Swap Test (Click to View Protocol Trace)

VCONN_SWAP_TO_ON_SUPPORTED is not set to YES

PASS 56. TD.4.10.6 Sink Alternate Mode Test (Click to View Protocol Trace)

PASS Step - 2: FSM_State_Disabled -> FSM_State_Unattached_SRC:

PASS Step - 3: FSM_State_Unattached_SRC -> FSM_State_AttachWait_SRC:

PASS Step - 4: FSM_State_AttachWait_SRC -> FSM_State_Attached_SRC:

PASS Step - 8 : Validate PD contract:

PASS Step - 11 : VDM Validation:

Model Operation Supported field set to NO

PASS Step - 14 : PUT's transition to disable:

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PASS 57. TD.4.11.1 DR Swap Test (Click to View Protocol Trace)

PASS Step-2: FSM_State_Disabled -> FSM_State_Unattached_SRC:

PASS Step-5: FSM_State_Unattached_SRC -> FSM_State_AttachWait_SRC:

PASS PUT transition to Attached.SNK:

Validation time range : 3.981sec to 3.984sec

Expected voltage in PORTA_CC1_VOLTAGE: Min = 0.25V and Max = 2.45V .Obtained voltage = 1.043V

PASS Step-6: FSM_State_AttachWait_SRC -> FSM_State_Attached_SRC:

Min= 100ms - Max = 475ms. Obtained time difference is 210.098ms

PASS Step-8 : DR swap validation:

DR_Swap initiated at 5.601S

PASS Step-7 : PUT's Vconn validation:

Expected voltage: 0V - 3V. Obtained voltage: 0.009V

Start time: 5.606S and stop time: 15.206S

PASS Step-10 : DR swap validation:

DR_Swap initiated at 5.608S

PASS Step-11: FSM_State_Attached_SRC -> FSM_State_Disabled:

PASS Step-12: FSM_State_Disabled -> FSM_State_Unattached_SNK:

PASS Step-12: Attach:

PASS PUT transition to Attached.SRC:

Validation time range : 16.444sec to 16.692sec

Expected voltage in PORTA_CC1_VOLTAGE: Min = 0.25V and Max = 2.45V .Obtained voltage = 0.304V

PASS Step-13: FSM_State_Unattached_SNK -> FSM_State_AttachWait_SNK:

PASS Step-13: FSM_State_AttachWait_SNK -> FSM_State_Attached_SNK:

PASS Step-14 : DR swap validation:

DR_Swap initiated at 10.206S

PASS Step-18 : DR swap validation:

DR_Swap initiated at 18.416S

PASS : FSM_State_Attached_SNK -> FSM_State_Disabled:

PASS 58. TD.4.11.2 Sink Dead Battery Test (Click to View Protocol Trace)

PASS Step - 5: FSM_State_Disabled -> FSM_State_Unattached_SRC:

PASS Step - 7: FSM_State_Unattached_SRC -> FSM_State_AttachWait_SRC:

PASS Step-10 : PUT draws current up to 500mA:

Validation time range : 3.701sec to 4.298sec

Expected current in PORTA_VBUS_CURRENT: Min = 0A

and Max = 0.5A .Obtained current = 0.028A

PASS Step - 8 : CVS presents VBUS:

PASS Step - 11: FSM_State_Attached_SRC -> FSM_State_Disabled:

NA 59. TD.4.12.2 Hub Port Types Test (Click to View Protocol Trace)

VIF field TYPE_C_PORT_ON_HUB is not set to YES

NA 60. TD.4.13.5 Cable EnterUSB and Data Reset Test (Click to View Protocol Trace)

USB4_Supported is not set to YES

Product_Type is not set to Cable

DUT Information

Manufacturer	Shenzhen Huafurui Technology Co., Ltd.
Model Number	P90
Serial Number	1

Test Information

Test Lab	Shenzhen BCTC Testing Co., Ltd.
Test_Engineer	Willem Wang
Remarks	Remarks
Date_and_Time	2025/6/7 15:29:56

Controller and Instrument Information

Parameter	Value
GRL_USB_PD_Controller_Serial_No	GRL-C2-EPR-2024150
GRL_USB_PD_Software_Version	1.6.31.0
GRL_USB_PD_Firmware_Version	1.2.85
GRL USB-PD Ethernet Buffer Size	62K
GRL USB-PD Eload Firmware Version	1.5 / 1.5
GRL USB-PD PPS Firmware Version	4.0 / 4.0
Calibration	Calibration Success
RX mask Power selection	Neutral Power
Device_Type	DRP
Cable Type	GRL_SPL_EPR_CABLE_1
Impedance (milli ohm)	11
FUNCTIONAL_TESTS CTS Version	v0.90
USB_PD_Spec Version	Rev3.2 Ver1.1RC2
USB_Type_C_Spec Version	v2.3 Oct-2023
VIF_File_Name	Smart-Phone__P90__1.1__0.xml
Noise Pattern Generation:	Two-Tone Noise
Application mode	Informational
Disabled all Pop-up during test execution	False
Pop-up Timer	0
Rerun Enabled	False
Rerun Count	1
Rerun Iteration	0
UI Live Update	False
Execution Time(In Minutes)	12

USB-C Functional Tests Information

Parameter	Value
Enable USB Data validation	Disabled
Is Dead Battery connected to PUT	Enabled
Number of USB Type-C Ports	0
Number of USB Type-B or Micro-B Ports or Type-A plug	0
Connected Hub is Embedded	Disabled

Product Capabilities

Parameter	VendorInfoFile	GetCapabilities
VIF_Specification	3.32	
Vendor_Name	Smartphone	
Model_Part_Number	P90	
Product_Revision	1.1	
TID	0	
VIF_Product_Type	Port Product	
Certification_Type	End Product	
Port_Label	0	
Connector_Type	Type-C®	
USB4_Supported	NO	
USB_PD_Support	YES	
PD_Port_Type	DRP	
Type_C_State_Machine	DRP	
Port_Battery_Powered	YES	
BC_1_2_Support	None	
Captive_Cable	NO	
PD_Spec_Revision_Major	3	
PD_Spec_Revision_Minor	1	
PD_Spec_Version_Major	1	
PD_Spec_Version_Minor	8	
PD_Specification_Revision	Revision 3	
SOP_Capable	YES	
SOP_P_Capable	NO	
SOP_PP_Capable	NO	
SOP_P_Debug_Capable	NO	
SOP_PP_Debug_Capable	NO	
Manufacturer_Info_Supported_Port	YES	
Manufacturer_Info_VID_Port	29CF	
Manufacturer_Info_PID_Port	5081	
Chunking_Implemented_SOP	YES	
Unchunked_Extended_Messages_Supported	NO	
Security_Msgs_Supported_SOP	NO	
Unconstrained_Power	NO	
Num_Fixed_Batteries	1	

Num_Swappable_Battery_Slots	0	
ID_Header_Connector_Type_SOP	USB Type-C® Receptacle	
USB_Comms_Capable	YES	
DR_Swap_To_DFP_Supported	YES	
DR_Swap_To_UFP_Supported	YES	
VCONN_Swap_To_On_Supported	NO	
VCONN_Swap_To_Off_Supported	NO	
Responds_To_Discov_SOP_UFP	YES	
Responds_To_Discov_SOP_DFP	YES	
Attempts_Discov_SOP	YES	
Power_Interruption_Available	No Interruption Possible	
Data_Reset_Supported	NO	
Enter_USB_Supported	NO	
Type_C_Can_Act_As_Host	YES	
Type_C_Can_Act_As_Device	YES	
Type_C_Implements_Try_SRC	NO	
Type_C_Implements_Try_SNK	YES	
Type_C_Supports_Audio_Accessory	YES	
Type_C_Is_VCONN_Powered_Accessory	NO	
Type_C_Is_Debug_Target_SRC	YES	
Type_C_Is_Debug_Target_SNK	YES	
RP_Value	Default	
Type_C_Port_On_Hub	NO	
Type_C_Power_Source	Both	
Type_C_Sources_VCONN	NO	
Type_C_Is_Alt_Mode_Controller	NO	
Type_C_Is_Alt_Mode_Adapter	NO	
Product_Total_Source_Power_mW	5000	
Port_Source_Power_Type	Assured	
Host_Supports_USB_Data	YES	
Host_Speed	USB 2	
Host_Contains_Captive_Retimer	NO	
Host_Is_Embedded	YES	
Host_Suspend_Supported	NO	
Is_DFP_On_Hub	NO	
Device_Supports_USB_Data	1	
Device_Speed	USB 2	
Device_Max_USB2_Speed	High Speed	
Device_Contains_Captive_Retimer	NO	
EPR_Supported_As_Src	NO	
FR_Swap_Type_C_Current_Capability_As_Initial_Sink	FR_Swap not supported	
Master_Port	YES	
Has_Invariant_PDOs	YES	
Port_Managed_Guaranteed_Type	Guaranteed Capability	
EPR_Supported_As_Snk	NO	
Accepts_PR_Swap_As_Src	YES	

Accepts_PR_Swap_As_Snk	YES	
Requests_PR_Swap_As_Src	NO	
Requests_PR_Swap_As_Snk	NO	
FR_Swap_Supported_As_Initial_Sink	NO	
XID_SOP	0	
Data_Capable_As_USB_Host_SOP	YES	
Data_Capable_As_USB_Device_SOP	YES	
Product_Type_UFP_SOP	PDUSB Peripheral	
Product_Type_DFP_SOP	PDUSB Host	
DFP_VDO_Port_Number	0	
Modal_Operation_Supported_SOP	NO	
USB_VID_SOP	344F	
PID_SOP	0000	
bcdDevice_SOP	0000	
PD_Power_As_Source	5000	
USB_Suspend_May_Be_Cleared	YES	
Sends_Pings	NO	
Num_Src_PDOs	1 Src PDO	
PD_OC_Protection	NO	
PD_Power_As_Sink	18000	
No_USB_Suspend_May_Be_Set	YES	
GiveBack_May_Be_Set	NO	
Higher_Capability_Set	NO	
FR_Swap_Reqd_Type_C_Current_As_Initial_Source	FR_Swap not supported	
Num_Snk_PDOs	2 Snk PDOs	

Source Capabilities

Parameter	VendorInfoFile	GetCapabilities
Src_PDO_Supply_Type #1	Fixed	
Src_PDO_Peak_Current #1	100% IOC	
Src_PDO_Voltage #1	5000 mV	
Src_PDO_Max_Current #1	1000 mA	

Sink Capabilities

Parameter	VendorInfoFile	GetCapabilities
Snk_PDO_Supply_Type #1	Fixed	
Snk_PDO_Voltage #1	5000 mV	
Snk_PDO_Op_Current #1	2000 mA	
Snk_PDO_Supply_Type #2	Fixed	
Snk_PDO_Voltage #2	9000 mV	
Snk_PDO_Op_Current #2	2000 mA	

DUT Max Power

Power	NA