Appendix

Report No.:	BCTC2504902986-1E
Applicant:	Shenzhen Huafurui Technology Co., Ltd.
Product Name:	Smartphone
Test Model:	P90
Tested Date:	2025-04-07 to 2025-06-11

Shenzhen BCTC Testing Co., Ltd.

C2-EPR Compliance Test Report

Test Summary - Overall

Total	Selected	PASS	FAIL	PASS Rate(%)	INCOMPLETE	NA	WARNING	NOT_SELECTED	ABORTED	NOT_EXECUTED
154	154	102	0	100%	0	52	0	0	0	0

Test Summary - All MOI

MOI Name	Total	PASS	FAIL	PASS Rate(%)	INCOMPLETE	NA	WARNING	NOT_SELECTED	ABORTED	NOT_EXECUTED
Power Delivery 3.2 Tests	154	102	0	100%	0	52	0	0	0	0

Power Delivery 3.2 Tests- Result Summary

Sl No	Test ID	Test Name	Test Result
1	TEST.PD.PHY.ALL.1	TEST.PD.PHY.ALL.1 Transmit Bit Rate and the Drift	PASS
2	TEST.PD.PHY.ALL.2	TEST.PD.PHY.ALL.2 Transmitter Eye Diagram	PASS
3	TEST.PD.PHY.ALL.3	TEST.PD.PHY.ALL.3 Collision Avoidance	PASS
4	TEST.PD.PHY.ALL.4	TEST.PD.PHY.ALL.4 Bus Idle Detection	PASS
5	TEST.PD.PHY.ALL.5	TEST.PD.PHY.ALL.5 Receiver Interference Rejection	PASS
6	TEST.PD.PHY.ALL.6	TEST.PD.PHY.ALL.6 Invalid SOP*	PASS
7	TEST.PD.PHY.ALL.7	TEST.PD.PHY.ALL.7 Valid SOP*	PASS
8	TEST.PD.PHY.ALL.8	TEST.PD.PHY.ALL.8 Incorrect CRC	PASS
9	TEST.PD.PHY.ALL.9	TEST.PD.PHY.ALL.9 Receiver Input Impedance	PASS
10	TEST.PD.PHY.PORT.1	TEST.PD.PHY.PORT.1 Invalid Reset Signals	PASS
11	TEST.PD.PROT.ALL.1	TEST.PD.PROT.ALL.1 Corrupted GoodCRC	PASS
12	TEST.PD.PROT.ALL.2	TEST.PD.PROT.ALL.2 Soft Reset and Hard Reset	PASS
13	TEST.PD.PROT.ALL.3	TEST.PD.PROT.ALL.3 Soft Reset response	PASS
14	TEST.PD.PROT.ALL.4	TEST.PD.PROT.ALL.4 Reset Signals and MessageID	PASS
15	TEST.PD.PROT.ALL.5	TEST.PD.PROT.ALL.5 Unrecognized Message	PASS
16	TEST.PD.PROT.ALL3.1	TEST.PD.PROT.ALL3.1 Get_Status Response	PASS
17	TEST.PD.PROT.ALL3.2	TEST.PD.PROT.ALL3.2 Get_Manufacturer_Info Response	PASS
18	TEST.PD.PROT.ALL3.3	TEST.PD.PROT.ALL3.3 Invalid Manufacturer Info Target	PASS
19	TEST.PD.PROT.ALL3.4	TEST.PD.PROT.ALL3.4 Invalid Manufacturer Info Ref	PASS
20	TEST.PD.PROT.ALL3.5	TEST.PD.PROT.ALL3.5 Chunked Extended Message Response	PASS
21	TEST.PD.PROT.ALL3.6	TEST.PD.PROT.ALL3.6 ChunkSenderResponseTimer Timeout	PASS
22	TEST.PD.PROT.ALL3.7	TEST.PD.PROT.ALL3.7 Security Messages Supported	PASS
23	TEST.PD.PROT.ALL3.8	TEST.PD.PROT.ALL3.8 Get Revision Response	PASS
24	TEST.PD.PROT.PORT3.1	TEST.PD.PROT.PORT3.1 Get Battery Status Response	PASS
25	TEST.PD.PROT.PORT3.2	TEST.PD.PROT.PORT3.2 Invalid Battery Status	PASS
26	TEST.PD.PROT.PORT3.3	TEST.PD.PROT.PORT3.3 Get Battery Cap Response	PASS
27	TEST.PD.PROT.PORT3.4	TEST.PD.PROT.PORT3.4 Invalid Battery Capabilities	PASS

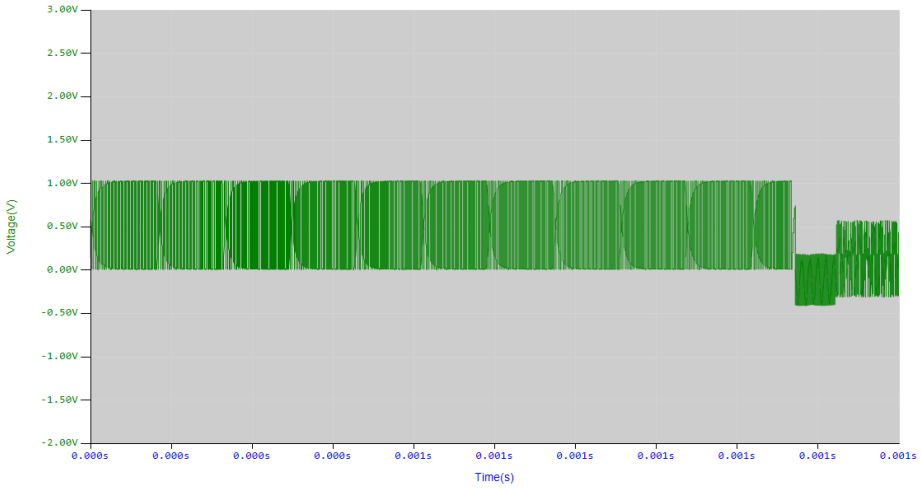
		Reference	
28	TEST.PD.PROT.PORT3.5	TEST.PD.PROT.PORT3.5 Get Country Codes Response	PASS
29	TEST.PD.PROT.PORT3.6	TEST.PD.PROT.PORT3.6 Get Country Info Response	PASS
30	TEST.PD.PROT.PORT3.7	TEST.PD.PROT.PORT3.7 Unchunked Extended Message Supported	NA
31	TEST.PD.PROT.SRC.1	TEST.PD.PROT.SRC.1 Get_Source_Cap Response	PASS
32	TEST.PD.PROT.SRC.2	TEST.PD.PROT.SRC.2 Get_Source_Cap No Request	PASS
33	TEST.PD.PROT.SRC.3	TEST.PD.PROT.SRC.3 Sender Response Timer Deadline	PASS
34	TEST.PD.PROT.SRC.4	TEST.PD.PROT.SRC.4 Reject Request	PASS
35	TEST.PD.PROT.SRC.5	TEST.PD.PROT.SRC.5 Reject Request Invalid Object Position	PASS
36	TEST.PD.PROT.SRC.6	TEST.PD.PROT.SRC.6 Atomic Message Sequence – Request	PASS
37	TEST.PD.PROT.SRC.7	TEST.PD.PROT.SRC.7 DR_Swap	PASS
38	TEST.PD.PROT.SRC.8	TEST.PD.PROT.SRC.8 VCONN_Swap Response	PASS
39	TEST.PD.PROT.SRC.9	TEST.PD.PROT.SRC.9 PR_Swap Response	PASS
40	TEST.PD.PROT.SRC.10	TEST.PD.PROT.SRC.10 PR_Swap – PSSourceOnTimer Timeout	PASS
41	TEST.PD.PROT.SRC.11	TEST.PD.PROT.SRC.11 Unexpected Message Received in Ready State	PASS
42	TEST.PD.PROT.SRC.12	TEST.PD.PROT.SRC.12 Get_Sink_Cap Response	PASS
43	TEST.PD.PROT.SRC.13	TEST.PD.PROT.SRC.13 PR Swap GoodCRC not sent in Response to PS_RDY	PASS
44	TEST.PD.PROT.SRC3.1	TEST.PD.PROT.SRC3.1 SourceCapabilityTimer Timeout	PASS
45	TEST.PD.PROT.SRC3.2	TEST.PD.PROT.SRC3.2 SenderResponseTimer Timeout	PASS
46	TEST.PD.PROT.SRC3.3	TEST.PD.PROT.SRC3.3 Get_Source_Cap_Extended Response	PASS
47	TEST.PD.PROT.SRC3.4	TEST.PD.PROT.SRC3.4 Alert Response Source Input Change	PASS
48	TEST.PD.PROT.SRC3.5	TEST.PD.PROT.SRC3.5 Alert Response Battery Status Change	PASS
49	TEST.PD.PROT.SRC3.6	TEST.PD.PROT.SRC3.6 Soft_Reset Sent when SinkTxOK	PASS
50	TEST.PD.PROT.SRC3.7	TEST.PD.PROT.SRC3.7 Get_PPS_Status Response	NA
51	TEST.PD.PROT.SRC3.8	TEST.PD.PROT.SRC3.8 SourcePPSCommTimer Deadline	NA
52	TEST.PD.PROT.SRC3.9	TEST.PD.PROT.SRC3.9 SourcePPSCommTimer Timeout	NA
53	TEST.PD.PROT.SRC3.10	TEST.PD.PROT.SRC3.10 SourcePPSCommTimer Stopped	NA
54	TEST.PD.PROT.SRC3.11	TEST.PD.PROT.SRC3.11 GoodCRC Specification Revision Compatibility	PASS
55	TEST.PD.PROT.SRC3.12	TEST.PD.PROT.SRC3.12 FR Swap Without Signaling	PASS
56	TEST.PD.PROT.SRC3.13	TEST.PD.PROT.SRC3.13 Cable Type Detection	PASS
57	TEST.PD.PROT.SRC3.14	TEST.PD.PROT.SRC3.14 Source Info	PASS
58	TEST.PD.PROT.SRC3.15	TEST.PD.PROT.SRC3.15 Alert Response Extended Alert	PASS
59	TEST.PD.PROT.SNK.1	TEST.PD.PROT.SNK.1 Get_Sink_Cap Response	PASS
60	TEST.PD.PROT.SNK.2	TEST.PD.PROT.SNK.2 Get_Source_Cap Response	PASS
61	TEST.PD.PROT.SNK.3	TEST.PD.PROT.SNK.3 SinkWaitCapTimer Deadline	PASS
62	TEST.PD.PROT.SNK.4	TEST.PD.PROT.SNK.4 SinkWaitCapTimer Timeout	PASS
63	TEST.PD.PROT.SNK.5	TEST.PD.PROT.SNK.5 SenderResponseTimer Deadline	PASS
64	TEST.PD.PROT.SNK.6	TEST.PD.PROT.SNK.6 SenderResponseTimer Timeout	PASS
65	TEST.PD.PROT.SNK.7	TEST.PD.PROT.SNK.7 PSTransitionTimer Timeout	PASS

66	TEST.PD.PROT.SNK.8	TEST.PD.PROT.SNK.8 Atomic Message Sequence – Accept	PASS
67	TEST.PD.PROT.SNK.9	TEST.PD.PROT.SNK.9 Atomic Message Sequence – PS_RDY	PASS
68	TEST.PD.PROT.SNK.10	TEST.PD.PROT.SNK.10 DR_Swap Request	PASS
69	TEST.PD.PROT.SNK.11	TEST.PD.PROT.SNK.11 VCONN_Swap Request	PASS
70	TEST.PD.PROT.SNK.12	TEST.PD.PROT.SNK.12 PR_Swap – PSSourceOffTimer Timeout	PASS
71	TEST.PD.PROT.SNK.13	TEST.PD.PROT.SNK.13 PR_Swap – Request SenderResponseTimer Timeout	PASS
72	TEST.PD.PROT.SNK.14	TEST.PD.PROT.SNK.14 Valid Use of GoodCRC on Power up	PASS
73	TEST.PD.PROT.SNK3.1	TEST.PD.PROT.SNK3.1 Get_Source_Cap_Extended	PASS
74	TEST.PD.PROT.SNK3.2	TEST.PD.PROT.SNK3.2 Alert Response Source Input Change	PASS
75	TEST.PD.PROT.SNK3.3	TEST.PD.PROT.SNK3.3 Alert Response Battery Status Change	PASS
76	TEST.PD.PROT.SNK3.4	TEST.PD.PROT.SNK3.4 Soft_Reset Sent Regardless of Rp Value	PASS
77	TEST.PD.PROT.SNK3.5	TEST.PD.PROT.SNK3.5 Sink PPS Normal Operation	PASS
78	TEST.PD.PROT.SNK3.6	TEST.PD.PROT.SNK3.6 Revision Number Test	PASS
79	TEST.PD.PROT.SNK3.7	TEST.PD.PROT.SNK3.7 GoodCRC Specification Revision Compatibility	PASS
80	TEST.PD.PROT.SNK3.9	TEST.PD.PROT.SNK3.9 Alert Response Extended Alert	PASS
81	TEST.PD.VDM.SNK.1	TEST.PD.VDM.SNK.1 Discovery Process and Enter Mode	PASS
82	TEST.PD.VDM.SNK.2	TEST.PD.VDM.SNK.2 Exit Mode without Entering	PASS
83	TEST.PD.VDM.SNK.5	TEST.PD.VDM.SNK.5 DR Swap in Modal Operation	PASS
84	TEST.PD.VDM.SNK.6	TEST.PD.VDM.SNK.6 Structured VDM Revision Number Test	PASS
85	TEST.PD.VDM.SNK.7	TEST.PD.VDM.SNK.7 Unrecognized VID in Unstructured VDM	PASS
86	TEST.PD.VDM.CBL.1	TEST.PD.VDM.CBL.1 Discovery Process and Enter Mode	NA
87	TEST.PD.VDM.SRC.1	TEST.PD.VDM.SRC.1 Discovery Process and Enter Mode	PASS
88	TEST.PD.VDM.SRC.2	TEST.PD.VDM.SRC.2 Invalid Fields – Discover Identity	PASS
89	TEST.PD.VDM.CBL3.1	TEST.PD.VDM.CBL3.1 Revision Number Test	NA
90	TEST.PD.PS.SRC.1	TEST.PD.PS.SRC.1 Multiple Request Messages	PASS
91	TEST.PD.PS.SRC.2	TEST.PD.PS.SRC.2 PDO Transition	PASS
92	TEST.PD.PS.SRC.3	TEST.PD.PS.SRC.3 Initial Source PDO Transition Post PR Swap	PASS
93	TEST.PD.PS.SRC.4	TEST.PD.PS.SRC.4 Source Behavior with Capability Mismatch Bit	PASS
94	TEST.PD.PS.SRC.5	TEST.PD.PS.SRC.5 Source Hard Reset Test	PASS
95	TEST.PD.PS.SNK.1	TEST.PD.PS.SNK.1 PDO Transition	PASS
96	TEST.PD.PS.SNK.2	TEST.PD.PS.SNK.2 Initial Sink PDO Transition	PASS
97	TEST.PD.PS.SNK.3	TEST.PD.PS.SNK.3 Multiple Request Load Test Post PR Swap	PASS
98	TEST.PD.EPR.SRC3.1	TEST.PD.EPR.SRC3.1 EPR Entry Process - UUT as VCONN Source	PASS
99	TEST.PD.EPR.SRC3.2	TEST.PD.EPR.SRC3.2 EPR Entry Process - Tester as VCONN Source	NA
100	TEST.PD.EPR.SRC3.3	TEST.PD.EPR.SRC3.3 EPR Entry failed - EPR Mode Capable bit not set in RDO	NA

101	TEST.PD.EPR.SRC3.4	TEST.PD.EPR.SRC3.4 EPR Entry failed – Tester as VCONN source	NA
102	TEST.PD.EPR.SRC3.5	TEST.PD.EPR.SRC3.5 EPR Entry Failed - EPR_Mode(Reserved) message	NA
103	TEST.PD.EPR.SRC3.6	TEST.PD.EPR.SRC3.6 EPR Entry Failed - Cable not EPR capable	NA
104	TEST.PD.EPR.SRC3.7	TEST.PD.EPR.SRC3.7 EPR Entry Failed - Interrupted by EPR_Get_Sink_Cap message	NA
105	TEST.PD.EPR.SRC3.8	TEST.PD.EPR.SRC3.8 EPR mode - Request message response	NA
106	TEST.PD.EPR.SRC3.9	TEST.PD.EPR.SRC3.9 EPR mode - EPR_Get_Source_Cap message	NA
107	TEST.PD.EPR.SRC3.10	TEST.PD.EPR.SRC3.10 SPR mode - EPR_Get_Source_Cap message	PASS
108	TEST.PD.EPR.SRC3.11	TEST.PD.EPR.SRC3.11 EPR Mode Exit by EPR_Mode_Exit message	NA
109	TEST.PD.EPR.SRC3.12	TEST.PD.EPR.SRC3.12 EPR mode - Get_Source_Cap message and Request message response	NA
110	TEST.PD.EPR.SRC3.13	TEST.PD.EPR.SRC3.13 EPR mode - tSourceEPRKeepAlive Timeout	NA
111	TEST.PD.EPR.SRC3.14	TEST.PD.EPR.SRC3.14 EPR mode - EPR_Request with Incorrect copy of PDO	NA
112	TEST.PD.EPR.SRC3.15	TEST.PD.EPR.SRC3.15 DiscoverIdentityCounter and DiscoverIdentityTimer check for SOP1	NA
113	TEST.PD.EPR.SRC3.16	TEST.PD.EPR.SRC3.16 PR_Swap for the UUT as EPR Source	NA
114	TEST.PD.EPR.SNK3.1	TEST.PD.EPR.SNK3.1 EPR Entry Process - Success	PASS
115	TEST.PD.EPR.SNK3.2	TEST.PD.EPR.SNK3.2 EPR Entry Fail tEnterEPR Timer Timeout	NA
116	TEST.PD.EPR.SNK3.3	TEST.PD.EPR.SNK3.3 EPR Fail by EPR Enter Failed Message	NA
117	TEST.PD.EPR.SNK3.4	TEST.PD.EPR.SNK3.4 EPR Entry Fail tFirstSourceCap Timer Timeout	NA
118	TEST.PD.EPR.SNK3.5	TEST.PD.EPR.SNK3.5 EPR Exit by Incorrect EPR Source Cap	NA
119	TEST.PD.EPR.SNK3.6	TEST.PD.EPR.SNK3.6 EPR Exit by EPR Exit Message	NA
120	TEST.PD.EPR.SNK3.8	TEST.PD.EPR.SNK3.8 EPR Exit by Source Cap Message	NA
121	TEST.PD.EPR.SNK3.9	TEST.PD.EPR.SNK3.9 EPR Entry failed due to SourceCap	NA
122	TEST.PD.EPR.SNK3.10	TEST.PD.EPR.SNK3.10 EPR Exit fail due to SinkWaitCapTimer timeout	NA
123	TEST.PD.EPR.SNK3.11	TEST.PD.EPR.SNK3.11 PR_Swap for the UUT as the EPR Sink	NA
124	TEST.PD.PS.EPR.SRC3.1	TEST.PD.PS.EPR.SRC3.1 Multiple EPR Request Load Test	NA
125	TEST.PD.PS.EPR.SRC3.2	TEST.PD.PS.EPR.SRC3.2 PDO Transitions in EPR Mode	NA
126	TEST.PD.FRS.SRC3.1	TEST.PD.FRS.SRC3.1 Normal Conditions	NA
127	TEST.PD.FRS.SRC3.2	TEST.PD.FRS.SRC3.2 Provider Only Checks	NA
128	TEST.PD.FRS.SRC3.3	TEST.PD.FRS.SRC3.3 GoodCRC Not Sent In Response To Accept	NA
129	TEST.PD.FRS.SRC3.4	TEST.PD.FRS.SRC3.4 GoodCRC Not Sent In Response To PS_RDY	NA
130	TEST.PD.FRS.SRC3.5	TEST.PD.FRS.SRC3.5 PSSourceOnTimer Deadline	NA

131	TEST.PD.FRS.SRC3.6	TEST.PD.FRS.SRC3.6 PSSourceOnTimer Timeout	NA
132	TEST.PD.FRS.SNK3.1	TEST.PD.FRS.SNK3.1 Normal Conditions	PASS
133	TEST.PD.FRS.SNK3.2	TEST.PD.FRS.SNK3.2 Normal Conditions, Consumer Only	NA
134	TEST.PD.FRS.SNK3.3	TEST.PD.FRS.SNK3.3 FR_Swap Not Sent	PASS
135	TEST.PD.FRS.SNK3.4	TEST.PD.FRS.SNK3.4 SendResponseTimer Timeout	PASS
136	TEST.PD.FRS.SNK3.5	TEST.PD.FRS.SNK3.5 PSSourceOffTimer Deadline	PASS
137	TEST.PD.FRS.SNK3.6	TEST.PD.FRS.SNK3.6 PSSourceOffTimer Timeout	PASS
138	TEST.PD.FRS.SNK3.7	TEST.PD.FRS.SNK3.7 GoodCRC Not Sent in Response to PS_RDY	PASS
139	TEST.PD.USB4.DRST.1	TEST.PD.USB4.DRST.1 –Data_Reset command response of UFP UUT	PASS
140	TEST.PD.USB4.DRST.2	TEST.PD.USB4.DRST.2 –Data_Reset command response of UFP UUT, Invalid Sequence	NA
141	TEST.PD.USB4.DRST.3	TEST.PD.USB4.DRST.3 –Data_Reset command response of UFP UUT Sourcing Vconn	NA
142	TEST.PD.USB4.DRST.4	TEST.PD.USB4.DRST.4 –DataReset command response of UFP UUT Sourcing Vconn – Invalid Sequence	NA
143	TEST.PD.USB4.DRST.5	TEST.PD.USB4.DRST.5 –Data_Reset command response of DFP UUT Sourcing Vconn	NA
144	TEST.PD.USB4.DRST.6	TEST.PD.USB4.DRST.6 –Data_Reset command response of DFP UUT, UFP Sourcing Vconn	NA
145	TEST.PD.USB4.DRST.7	TEST.PD.USB4.DRST.7 –Data_reset command response of DFP UUT, UFP Sourcing Vconn- VCONNDischargeTimer expiry check	NA
146	TEST.PD.USB4.EUSB.1	TEST.PD.USB4.EUSB.1 – Enter_USB Message response of UFP UUT-Valid Mode	NA
147	TEST.PD.USB4.EUSB.2	TEST.PD.USB4.EUSB.2 – Enter_USB Message response of UFP UUT-Invalid Mode	NA
148	TEST.PD.USB4.EUSB.3	TEST.PD.USB4.EUSB.3 – Enter_USB Flow-USB4 DFP Connected to USB4 UFP using an Active Cable	NA
149	TEST.PD.USB4.EUSB.4	TEST.PD.USB4.EUSB.4 – DR_Swap after Entering USB4 Mode entry	NA
150	TEST.PD.USB4.EUSB.5	TEST.PD.USB4.EUSB.5 – tEnterUSBWait check for USB4 DFP	NA
151	TEST.PD.USB4.CBL.1	TEST.PD.USB4.CBL.1 – Enter_USB Message response of cable UUT-Valid Mode	NA
152	TEST.PD.USB4.CBL.2	TEST.PD.USB4.CBL.2 – Enter_USB Message response of Cable UUT-Invalid Mode	NA
153	2.1	Common Checks	PASS
154	2.2	Common Procedures	PASS

BUS_IDLE_HSADC_0



Power Delivery 3.2 Tests - Detailed Test Result

Test Status	Test Description
	1. TEST.PD.PHY.ALL.1 Transmit Bit Rate and the Drift (Click to View Protocol Trace)
PASS	**1 / 1 captures completed**
	COMMON.PROC.BU.2:
PASS	
	COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:
PASS	
	SourceCap Packet17
	UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS	
	Request Packet19
	Rev3ChkdSnk:
PASS	
	fBitRateMeas - TEST.PD.PHY.ALL.1#1:
PASS	
	Bit Rate-1:
PASS	
	Valid Protocol response for BIST Request
	Bit Rate-2:
PASS	
	Valid BIST response pattern
	Bit Rate-3:
PASS	
	Bit Rate is 295.278 Kbps. Test limit (270 ~ 330) Kbps
	pBitRateMeas - TEST.PD.PHY.ALL.1#2:
PASS	
	Bit Rate-4:
PASS	
	Bit Rate is 0.013 %. Test limit: X < 0.25%
	tBISTContMode Limits validation - TEST.PD.PHY.ALL.1#3:
PASS	
	Bit Rate-5:

PASS

BIST pattern duration 35.0590649 mS [Limit : (30 ~ 60)ms]

2. TEST.PD.PHY.ALL.2 Transmitter Eye Diagram (Click to View Protocol Trace)

PASS

1/1 captures completed

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet17

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet19

Rev3ChkdSnk:

PASS

fBitRateMeas - TEST.PD.PHY.ALL.2#1:

PASS

Eye diagram-1:

PASS

Valid Protocol response for BIST Request

Eye diagram-2:

PASS

Valid BIST response pattern

Eye diagram-3:

PASS

Eye diagram plot passed at Mid Crossing Level + 10mV

pBitRateMeas - TEST.PD.PHY.ALL.2#2:

PASS

Eye diagram-4:

PASS

BIST pattern duration 34.8576319 mS [Limit : (30 ~ 60)ms]

BMC_PHY_TX_EYE_5:

PASS

Rise time:
Average value = 431.232858 nS
Minimum value = 414.394601 nS
Maximum value = 448.908490 nS
Minimum Limit = 300 ns

Fall time:
Average value = 477.728803 nS
Minimum value = 459.477802 nS
Maximum value = 495.768633 nS
Minimum Limit = 300 ns

3. TEST.PD.PHY.ALL.3 Collision Avoidance (Click to View Protocol Trace)

PASS

2/2 captures completed

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet16

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet18

Rev3ChkdSnk:

PASS

Packet32

Alternating 0's and 1's for 200us - TEST.PD.PHY.ALL.3#1:

PASS

Packet42

Continuous 0's for 195us - TEST.PD.PHY.ALL.3#2:

PASS

Packet52

4. TEST.PD.PHY.ALL.4 Bus Idle Detection (Click to View Protocol Trace)

PASS

1/1 captures completed

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet16

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet18

Rev3ChkdSnk:

PASS

First BIST message Packet 32

Check BusIdle - TEST.PD.PHY.ALL.4#1:

PASS

UUT respond GoodCRC to BIST_Test_Data

5. TEST.PD.PHY.ALL.5 Receiver Interference Rejection

PASS

4/4 captures completed

Rev3ChkdSnk:

PASS

TX Group 1 Noise Src - TEST.PD.PHY.ALL.5#1:

PASS

BIST count 13362 , GoodCRC count 13362

TX Group 2 Noise - TEST.PD.PHY.ALL.5#2:

PASS

BIST count 13362 , GoodCRC count 13362

Rev3ChkdSrc:

PASS

TX Group 1 Noise Snk - TEST.PD.PHY.ALL.5#1:

PASS

BIST count 13362 , GoodCRC count 13362

TX Group 3 Noise - TEST.PD.PHY.ALL.5#3:

PASS

BIST count 13362 , GoodCRC count 13362

6. TEST.PD.PHY.ALL.6 Invalid SOP* (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet16

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet18

Rev3ChkdSnk:

PASS

Check DUT Response - TEST.PD.PHY.ALL.6#1:

PASS

7. TEST.PD.PHY.ALL.7 Valid SOP* (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet17

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet19

Rev3ChkdSnk:

PASS

Check BIST Response for SOP - TEST.PD.PHY.ALL.7#2:

PASS

Check BIST Response for SOP1 - TEST.PD.PHY.ALL.7#3:

PASS

Check BIST Response for SOP2 - TEST.PD.PHY.ALL.7#5:

PASS

Check BIST Response for SOP1_Debug - TEST.PD.PHY.ALL.7#7:

PASS

Check BIST Response for SOP2_Debug - TEST.PD.PHY.ALL.7#8:

PASS

8. TEST.PD.PHY.ALL.8 Incorrect CRC (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet16

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet18

Rev3ChkdSnk:

PASS

Check Flip 0 on CRC before 4b5b encoding - TEST.PD.PHY.ALL.8#2:

PASS

Check Flip 0 on CRC after 4b5b encoding - TEST.PD.PHY.ALL.8#2:

PASS

Check Flip 0 on payload before 4b5b encoding -
PASS TEST.PD.PHY.ALL.8#2:

Check Flip 0 on payload after 4b5b encoding - TEST.PD.PHY.ALL.8#2:
PASS

Check replace third 5b symbol - TEST.PD.PHY.ALL.8#2:
PASS

9. TEST.PD.PHY.ALL.9 Receiver Input Impedance (Click to View
PASS Protocol Trace)

COMMON.PROC.BU.2:
PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:
PASS

SourceCap Packet16

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet18

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:
PASS

SourceCap Packet51

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet53

Rev3ChkdSnk:
PASS

Sink UUT voltage on the CC line - TEST.PD.PHY.ALL.9#1:
PASS

CC-line voltage is 1.05V at time 2.89079373s

Source UUT voltage on the CC line - TEST.PD.PHY.ALL.9#2:
PASS

Cable Plug voltage on the CC line - TEST.PD.PHY.ALL.9#3:
PASS

Rev3ChkdSnk:
PASS

Sink UUT voltage on the CC line - TEST.PD.PHY.ALL.9#4:
PASS

CC-line voltage is 1.05V at time 6.13679737s

Cable Plug voltage on the CC line [Without VCONN or VBUS] -
PASS TEST.PD.PHY.ALL.9#5:

10. TEST.PD.PHY.PORT.1 Invalid Reset Signals (Click to View Protocol
PASS Trace)

COMMON.PROC.BU.2:
PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:
PASS

SourceCap Packet16

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet18

Rev3ChkdSnk:
PASS

Check Response message - TEST.PD.PHY.PORT.1#1:

PASS

Check Response message - TEST.PD.PHY.PORT.1#2:

PASS

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 15.119s and SourceCap time: 15.307s at protocol index #116

[PASS] Max = 250ms. Obtained time difference is 188.315ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet120

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.064ms

Packet 122

Rev3ChkdSrc:

PASS

Check Response message - TEST.PD.PHY.PORT.1#1:

PASS

Check Response message - TEST.PD.PHY.PORT.1#2:

PASS

11. TEST.PD.PROT.ALL.1 Corrupted GoodCRC (Click to View Protocol Trace)

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:

PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet89

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet91

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 13.3s and SourceCap time: 13.485s at protocol index #185

[PASS] Max = 250ms. Obtained time difference is 185.815ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet189

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.218ms

Packet 191

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 18.85s and SourceCap time: 19.033s at protocol index #260

[PASS] Max = 250ms. Obtained time difference is 183.315ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet264

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.459ms

Packet 266

Rev2Snk:

PASS

GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.1#2:

PASS

SinkCap retransmit check - TEST.PD.PROT.ALL.1#5:

PASS

GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.1#7:

PASS

SinkCap retransmit check - TEST.PD.PROT.ALL.1#10:

PASS

SinkCap retransmit messageID check - TEST.PD.PROT.ALL.1#11:

PASS

Tester sent Get_Sink_Cap message

Packet 56

Tester sent Get_Source_Cap message

Packet 60

UUT SoftReset Check - TEST.PD.PROT.ALL.1#12:

PASS

UUT sent SoftReset message at protocol index 62

Rev3ChkdSnk:

PASS

GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.1#2:

PASS

SinkCap retransmit check - TEST.PD.PROT.ALL.1#5:

PASS

GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.1#7:

PASS

SinkCap retransmit check - TEST.PD.PROT.ALL.1#10:

PASS

SinkCap retransmit messageID check - TEST.PD.PROT.ALL.1#11:

PASS

Tester sent Get_Sink_Cap message

Packet 145
Tester sent Get_Source_Cap message
Packet 149
UUT SoftReset Check - TEST.PD.PROT.ALL.1#12:
PASS
UUT sent SoftReset message at protocol index 153
Rev2Src:
PASS
GetSinkCap response Source UUT - TEST.PD.PROT.ALL.1#3:
PASS
SinkCap retransmit check - TEST.PD.PROT.ALL.1#5:
PASS
GetSinkCap response Source UUT - TEST.PD.PROT.ALL.1#8:
PASS
SinkCap retransmit check - TEST.PD.PROT.ALL.1#10:
PASS
SinkCap retransmit messageID check - TEST.PD.PROT.ALL.1#11:
PASS
Tester sent Get_Sink_Cap message
Packet 227
Tester sent Get_Source_Cap message
Packet 231
UUT SoftReset Check - TEST.PD.PROT.ALL.1#12:
PASS
UUT sent SoftReset message at protocol index 233
Rev3ChkdSrc:
PASS
GetSinkCap response Source UUT - TEST.PD.PROT.ALL.1#3:
PASS
SinkCap retransmit check - TEST.PD.PROT.ALL.1#5:
PASS
GetSinkCap response Source UUT - TEST.PD.PROT.ALL.1#8:
PASS
SinkCap retransmit check - TEST.PD.PROT.ALL.1#10:
PASS
SinkCap retransmit messageID check - TEST.PD.PROT.ALL.1#11:
PASS
Tester sent Get_Sink_Cap message
Packet 300
Tester sent Get_Source_Cap message
Packet 304
UUT SoftReset Check - TEST.PD.PROT.ALL.1#12:
PASS
UUT sent SoftReset message at protocol index 306

12. TEST.PD.PROT.ALL.2 Soft Reset and Hard Reset (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:
PASS
COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:
PASS
SourceCap Packet14
UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet79

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet81

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 15.207s and SourceCap time: 15.393s at protocol index #163

[PASS] Max = 250ms. Obtained time difference is 185.815ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet167

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.22ms

Packet 169

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 21.737s and SourceCap time: 21.921s at protocol index #234

[PASS] Max = 250ms. Obtained time difference is 184.148ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet238

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.455ms

Packet 240

Rev2Snk:

PASS

GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#2:

PASS

UUT sent SinkCap at protocol index#27

GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#3:

PASS

UUT retransmit check - TEST.PD.PROT.ALL.2#5:

PASS

UUT retransmitted the SinkCap message 3 times at the protocol index 27.

SoftReset from UUT - TEST.PD.PROT.ALL.2#7:

PASS

UUT Response check - TEST.PD.PROT.ALL.2#8:
PASS

UUT sent Request message at protocol index : 38

GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#12:
PASS

UUT sent SinkCap at protocol index#47

GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#13:
PASS

UUT retransmit check - TEST.PD.PROT.ALL.2#15:
PASS

UUT retransmitted the SinkCap message 3 times at the protocol index 47.

SoftReset from UUT - TEST.PD.PROT.ALL.2#17:
PASS

UUT retransmit check - TEST.PD.PROT.ALL.2#18:
PASS

UUT retransmitted the SoftReset message 3 times at the protocol index 51.

UUT Hard Reset message check - TEST.PD.PROT.ALL.2#19:
PASS

UUT sent Hard_Reset message
Packet 55
[PASS] Max = 6.1ms. Obtained time difference is 2.888ms

Rev3ChkdSnk:
PASS

GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#2:
PASS

UUT sent SinkCap at protocol index#97

GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#3:
PASS

UUT retransmit check - TEST.PD.PROT.ALL.2#5:
PASS

UUT retransmitted the SinkCap message 2 times at the protocol index 97.

SoftReset from UUT - TEST.PD.PROT.ALL.2#7:
PASS

UUT Response check - TEST.PD.PROT.ALL.2#8:
PASS

UUT sent Request message at protocol index : 109

GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#12:
PASS

UUT sent SinkCap at protocol index#122

GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#13:
PASS

UUT retransmit check - TEST.PD.PROT.ALL.2#15:
PASS

UUT retransmitted the SinkCap message 2 times at the protocol index 122.

SoftReset from UUT - TEST.PD.PROT.ALL.2#17:
PASS

UUT retransmit check - TEST.PD.PROT.ALL.2#18:
PASS

UUT retransmitted the SoftReset message 2 times at the protocol index 127.

UUT Hard Reset message check - TEST.PD.PROT.ALL.2#19:

PASS

UUT sent Hard_Reset message
Packet 130
[PASS] Max = 6.1ms. Obtained time difference is 2.329ms

Rev2Src:

PASS

GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#2:

PASS

GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#3:

PASS

UUT is a DRP and sent SinkCap at the protocol index 177

UUT retransmit check - TEST.PD.PROT.ALL.2#5:

PASS

UUT retransmitted the SinkCap message 3 times at the protocol index 177.

SoftReset from UUT - TEST.PD.PROT.ALL.2#9:

PASS

UUT Response check - TEST.PD.PROT.ALL.2#10:

PASS

UUT sent Request message at protocol index : 187

GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#12:

PASS

GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#13:

PASS

UUT is a DRP and sent SinkCap at the protocol index 196

UUT retransmit check - TEST.PD.PROT.ALL.2#15:

PASS

UUT retransmitted the SinkCap message 3 times at the protocol index 196.

SoftReset from UUT - TEST.PD.PROT.ALL.2#17:

PASS

UUT retransmit check - TEST.PD.PROT.ALL.2#18:

PASS

UUT retransmitted the SoftReset message 3 times at the protocol index 200.

UUT Hard Reset message check - TEST.PD.PROT.ALL.2#19:

PASS

UUT sent Hard_Reset message
Packet 204
[PASS] Max = 6.1ms. Obtained time difference is 1.759ms

Rev3ChkdSrc:

PASS

GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#2:

PASS

GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#3:

PASS

UUT is a DRP and sent SinkCap at the protocol index 248

UUT retransmit check - TEST.PD.PROT.ALL.2#5:

PASS

UUT retransmitted the SinkCap message 2 times at the protocol index 248.

SoftReset from UUT - TEST.PD.PROT.ALL.2#9:

PASS

UUT Response check - TEST.PD.PROT.ALL.2#10:

PASS

UUT sent Request message at protocol index : 257

GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#12:

PASS

GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#13:

PASS

UUT is a DRP and sent SinkCap at the protocol index 266

UUT retransmit check - TEST.PD.PROT.ALL.2#15:

PASS

UUT retransmitted the SinkCap message 2 times at the protocol index 266.

SoftReset from UUT - TEST.PD.PROT.ALL.2#17:

PASS

UUT retransmit check - TEST.PD.PROT.ALL.2#18:

PASS

UUT retransmitted the SoftReset message 2 times at the protocol index 269.

UUT Hard Reset message check - TEST.PD.PROT.ALL.2#19:

PASS

UUT sent Hard_Reset message

Packet 272

[PASS] Max = 6.1ms. Obtained time difference is 3.202ms

13. TEST.PD.PROT.ALL.3 Soft Reset response (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:

PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet81

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet83

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 11.3s and SourceCap time: 11.479s at protocol

index #192

[PASS] Max = 250ms. Obtained time difference is 179.149ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet196

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 41.038ms

Packet 198

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 15.848s and SourceCap time: 16.036s at protocol index #268

[PASS] Max = 250ms. Obtained time difference is 188.315ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet272

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.101ms

Packet 274

Rev2Snk:

PASS

GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.3#2:

PASS

UUT is a DRP and it sent SinkCap message at the protocol index 27

GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#3:

PASS

Soft Reset message validation - TEST.PD.PROT.ALL.3#4:

PASS

UUT Request message check - TEST.PD.PROT.ALL.3#5:

PASS

DUT sent Request message at protocol index: 56

Source Capabilities message validation - TEST.PD.PROT.ALL.3#6:

PASS

GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#8:

PASS

DUT responded with SinkCap to Get_Sink_Cap at protocol index : 65

GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#9:

PASS

Rev3ChkdSnk:

PASS

GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.3#2:

PASS

UUT is a DRP and it sent SinkCap message at the protocol index 100

GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#3:

PASS

Soft Reset message validation - TEST.PD.PROT.ALL.3#4:
PASS
UUT Request message check - TEST.PD.PROT.ALL.3#5:
PASS
DUT sent Request message at protocol index: 157
Source Capabilities message validation - TEST.PD.PROT.ALL.3#6:
PASS
GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#8:
PASS
DUT responded with SinkCap to Get_Sink_Cap at protocol index
: 170
GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#9:
PASS
Rev2Src:
PASS
GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.3#2:
PASS
GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#3:
PASS
UUT is a DRP and it sent SinkCap message at the protocol index
206
Soft Reset message validation - TEST.PD.PROT.ALL.3#4:
PASS
UUT Request message check - TEST.PD.PROT.ALL.3#5:
PASS
Source Capabilities message validation - TEST.PD.PROT.ALL.3#6:
PASS
SourceCap message at protocol index: 240 received within the
250ms
GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#8:
PASS
GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#9:
PASS
DUT responded with SinkCap to Get_Sink_Cap at protocol index
: 251
Rev3ChkdSrc:
PASS
GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.3#2:
PASS
GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#3:
PASS
UUT is a DRP and it sent SinkCap message at the protocol index
282
Soft Reset message validation - TEST.PD.PROT.ALL.3#4:
PASS
UUT Request message check - TEST.PD.PROT.ALL.3#5:
PASS
Source Capabilities message validation - TEST.PD.PROT.ALL.3#6:
PASS
SourceCap message at protocol index: 316 received within the
250ms
GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#8:

PASS

GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#9:

PASS

DUT responded with SinkCap to Get_Sink_Cap at protocol index : 327

14. TEST.PD.PROT.ALL.4 Reset Signals and MessageID (Click to View

PASS Protocol Trace)

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:

PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet86

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet88

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 11.57s and SourceCap time: 11.752s at protocol index #216

[PASS] Max = 250ms. Obtained time difference is 182.482ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet220

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 39.416ms

Packet 222

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 16.246s and SourceCap time: 16.432s at protocol index #303

[PASS] Max = 250ms. Obtained time difference is 186.648ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet307

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.594ms

Packet 309

Rev2Snk:

PASS

Tester sent Hard_Reset message

Packet 49

Get Sink Cap response check - TEST.PD.PROT.ALL.4#2:

PASS

UUT initiated SinkCap for tester initiated Get_Sink_Capability, at protocol index 31

UUT Request check - TEST.PD.PROT.ALL.4#4:

PASS

UUT Responded with Request message at protocol index 53

Get Sink Cap response check - TEST.PD.PROT.ALL.4#9:

PASS

UUT initiated SinkCap for tester initiated Get_Sink_Capability, at protocol index 62

Get Sink Cap response check - TEST.PD.PROT.ALL.4#11:

PASS

UUT ignored tester initiated Get_Sink_Capability at protocol index 65

Get Sink Cap response check - TEST.PD.PROT.ALL.4#13:

PASS

UUT initiated SinkCap for tester initiated Get_Sink_Capability, at protocol index 70

Rev3ChkdSnk:

PASS

Tester sent Hard_Reset message

Packet 155

Get Sink Cap response check - TEST.PD.PROT.ALL.4#2:

PASS

UUT initiated SinkCap for tester initiated Get_Sink_Capability, at protocol index 114

UUT Request check - TEST.PD.PROT.ALL.4#4:

PASS

UUT Responded with Request message at protocol index 162

Get Sink Cap response check - TEST.PD.PROT.ALL.4#9:

PASS

UUT initiated SinkCap for tester initiated Get_Sink_Capability, at protocol index 176

Get Sink Cap response check - TEST.PD.PROT.ALL.4#11:

PASS

UUT ignored tester initiated Get_Sink_Capability at protocol index 184

Get Sink Cap response check - TEST.PD.PROT.ALL.4#13:

PASS

UUT initiated SinkCap for tester initiated Get_Sink_Capability, at protocol index 194

Rev2Src:

PASS

Tester sent Hard_Reset message

Packet 260

Get Sink Cap response check - TEST.PD.PROT.ALL.4#3:

PASS

UUT is a DRP and sent SinkCap at the protocol index 234

HardReset response check - TEST.PD.PROT.ALL.4#5:

PASS

Source Capability timing check - TEST.PD.PROT.ALL.4#6:

PASS

DUT initiate first source cap within 250ms. Obtained time difference is 159.15075ms

Get Sink Cap response check - TEST.PD.PROT.ALL.4#10:

PASS

UUT is a DRP and sent SinkCap at the protocol index 278

Get Sink Cap response check - TEST.PD.PROT.ALL.4#11:

PASS

UUT ignored tester initiated Get_Sink_Capability at protocol index 281

Get Sink Cap response check - TEST.PD.PROT.ALL.4#14:

PASS

UUT is a DRP and sent SinkCap at the protocol index 286

Rev3ChkdSrc:

PASS

Tester sent Hard_Reset message

Packet 348

Get Sink Cap response check - TEST.PD.PROT.ALL.4#3:

PASS

UUT is a DRP and sent SinkCap at the protocol index 321

HardReset response check - TEST.PD.PROT.ALL.4#5:

PASS

Source Capability timing check - TEST.PD.PROT.ALL.4#6:

PASS

DUT initiate first source cap within 250ms. Obtained time difference is 156.651009999997ms

Get Sink Cap response check - TEST.PD.PROT.ALL.4#10:

PASS

UUT is a DRP and sent SinkCap at the protocol index 366

Get Sink Cap response check - TEST.PD.PROT.ALL.4#11:

PASS

UUT ignored tester initiated Get_Sink_Capability at protocol index 369

Get Sink Cap response check - TEST.PD.PROT.ALL.4#14:

PASS

UUT is a DRP and sent SinkCap at the protocol index 374

15. TEST.PD.PROT.ALL.5 Unrecognized Message (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:

PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet43

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet45

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 7.259s and SourceCap time: 7.44s at protocol index #84

[PASS] Max = 250ms. Obtained time difference is 181.649ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet88

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.749ms

Packet 90

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 9.814s and SourceCap time: 10.002s at protocol index #115

[PASS] Max = 250ms. Obtained time difference is 187.481ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet119

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.351ms

Packet 121

Rev2Snk:

PASS

Source or Sink UUT Response Check - TEST.PD.PROT.ALL.5#2:

PASS

DUT responded with Reject message, Packet index : 27

Rev3ChkdSnk:

PASS

Source or Sink UUT Response Check - TEST.PD.PROT.ALL.5#2:

PASS

DUT responded with Not_Supported message, Packet index : 61

Rev2Src:

PASS

Source or Sink UUT Response Check - TEST.PD.PROT.ALL.5#2:

PASS

DUT responded with Reject message, Packet index : 98

Rev3ChkdSrc:

PASS

Source or Sink UUT Response Check - TEST.PD.PROT.ALL.5#2:

PASS

DUT responded with Not_Supported message, Packet index : 129

16. TEST.PD.PROT.ALL3.1 Get_Status Response (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet15

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet17

COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk:

PASS

SourceCap Packet57

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet59

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 7.387s and SourceCap time: 7.573s at protocol index #99

[PASS] Max = 250ms. Obtained time difference is 185.815ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet103

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.064ms

Packet 105

COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 9.973s and SourceCap time: 10.158s at protocol index #130

[PASS] Max = 250ms. Obtained time difference is 184.981ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet134

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.716ms

Packet 136

Rev3ChkdSnk:

PASS

Get_Status message response check - TEST.PD.PROT.ALL3.1#3:

PASS

DUT sent Not_Supported message for the Get_Status at protocol index 34

NA Status message field check - TEST.PD.PROT.ALL3.1#4:

DUT sent Not_Supported message for the Get_Status at protocol index 34

Rev3UnchkdSnk:

PASS

Get_Status message response check - TEST.PD.PROT.ALL3.1#3:

PASS

DUT sent Not_Supported message for the Get_Status at protocol index 76

NA Status message field check - TEST.PD.PROT.ALL3.1#4:

DUT sent Not_Supported message for the Get_Status at protocol index 76

Rev3ChkdSrc:

PASS

Get_Status message response check - TEST.PD.PROT.ALL3.1#3:

PASS

DUT sent Not_Supported message for the Get_Status at protocol index 113

NA Status message field check - TEST.PD.PROT.ALL3.1#4:

DUT sent Not_Supported message for the Get_Status at protocol index 113

Rev3UnchkdSrc:

PASS

Get_Status message response check - TEST.PD.PROT.ALL3.1#3:

PASS

DUT sent Not_Supported message for the Get_Status at protocol index 144

NA Status message field check - TEST.PD.PROT.ALL3.1#4:

DUT sent Not_Supported message for the Get_Status at protocol index 144

17. TEST.PD.PROT.ALL3.2 Get_Manufacturer_Info Response (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet15

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet17

COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk:

PASS

SourceCap Packet54

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet56

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 7.267s and SourceCap time: 7.452s at protocol index #94

[PASS] Max = 250ms. Obtained time difference is 184.148ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet98

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.149ms

Packet 100

COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 9.819s and SourceCap time: 10.003s at protocol index #125

[PASS] Max = 250ms. Obtained time difference is 184.148ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet129

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.739ms

Packet 131

Rev3ChkdSnk:

PASS

Response Check - TEST.PD.PROT.ALL3.2#2:

PASS

DUT sent Manufacturer_Info message for the Get_Manufacturer_Info at ptotocol index 33

VIF Check - TEST.PD.PROT.ALL3.2#3:

PASS

DUT decoded VID is 0x29cf and mentioned in VIF is 0x29cf

DUT decoded PID is 0x5081 and mentioned in VIF is 0x5081

Rev3UnchkdSnk:

PASS

Response Check - TEST.PD.PROT.ALL3.2#2:

PASS

DUT sent Manufacturer_Info message for the Get_Manufacturer_Info at ptotocol index 72

VIF Check - TEST.PD.PROT.ALL3.2#3:

PASS

DUT decoded VID is 0x29cf and mentioned in VIF is 0x29cf

DUT decoded PID is 0x5081 and mentioned in VIF is 0x5081

Rev3ChkdSrc:

PASS

Response Check - TEST.PD.PROT.ALL3.2#2:

PASS

DUT sent Manufacturer_Info message for the Get_Manufacturer_Info at ptotocol index 108

VIF Check - TEST.PD.PROT.ALL3.2#3:

PASS

DUT decoded VID is 0x29cf and mentioned in VIF is 0x29cf
DUT decoded PID is 0x5081 and mentioned in VIF is 0x5081

Rev3UnchkdSrc:

PASS

Response Check - TEST.PD.PROT.ALL3.2#2:

PASS

DUT sent Manufacturer_Info message for the Get_Manufacturer_Info at ptotocol index 139

VIF Check - TEST.PD.PROT.ALL3.2#3:

PASS

DUT decoded VID is 0x29cf and mentioned in VIF is 0x29cf
DUT decoded PID is 0x5081 and mentioned in VIF is 0x5081

18. TEST.PD.PROT.ALL3.3 Invalid Manufacturer Info Target (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet15

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet17

COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk:

PASS

SourceCap Packet54

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet56

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 7.273s and SourceCap time: 7.463s at protocol index #94

[PASS] Max = 250ms. Obtained time difference is 190.814ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet98

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 39.335ms
Packet 100

COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 9.817s and SourceCap time: 10.004s at protocol index #125

[PASS] Max = 250ms. Obtained time difference is 186.648ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet129

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.79ms

Packet 131

Rev3ChkdSnk:

PASS

Response Check - TEST.PD.PROT.ALL3.3#2:

PASS

DUT sent Manufacturer_Info message for the Get_Manufacturer_Info at protocol index #33

Manufacturer String Check - TEST.PD.PROT.ALL3.3#3:

PASS

DUT manufacture info string matched with specified format

Rev3UnchkdSnk:

PASS

Response Check - TEST.PD.PROT.ALL3.3#2:

PASS

DUT sent Manufacturer_Info message for the Get_Manufacturer_Info at protocol index #72

Manufacturer String Check - TEST.PD.PROT.ALL3.3#3:

PASS

DUT manufacture info string matched with specified format

Rev3ChkdSrc:

PASS

Response Check - TEST.PD.PROT.ALL3.3#2:

PASS

DUT sent Manufacturer_Info message for the Get_Manufacturer_Info at protocol index #108

Manufacturer String Check - TEST.PD.PROT.ALL3.3#3:

PASS

DUT manufacture info string matched with specified format

Rev3UnchkdSrc:

PASS

Response Check - TEST.PD.PROT.ALL3.3#2:

PASS

DUT sent Manufacturer_Info message for the Get_Manufacturer_Info at protocol index #139

Manufacturer String Check - TEST.PD.PROT.ALL3.3#3:

PASS

DUT manufacture info string matched with specified format

19. TEST.PD.PROT.ALL3.4 Invalid Manufacturer Info Ref (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:
PASS
COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:
PASS
SourceCap Packet15
UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS
Request Packet17
COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk:
PASS
SourceCap Packet54
UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS
Request Packet56
COMMON.PROC.BU.1:
PASS
COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:
PASS
First source capability timer - COMMON.PROC.BU.1#1:
PASS
Vbus up time: 7.269s and SourceCap time: 7.453s at protocol index #94
[PASS] Max = 250ms. Obtained time difference is 184.148ms
DUT responded with accept message - COMMON.PROC.BU.1#2:
PASS
Packet98
tSrcTransReq timer check - COMMON.PROC.BU.1#3:
PASS
[PASS] Max = 325ms. Obtained time difference is 39.408ms
Packet 100
COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc:
PASS
First source capability timer - COMMON.PROC.BU.1#1:
PASS
Vbus up time: 9.821s and SourceCap time: 10.008s at protocol index #125
[PASS] Max = 250ms. Obtained time difference is 187.481ms
DUT responded with accept message - COMMON.PROC.BU.1#2:
PASS
Packet129
tSrcTransReq timer check - COMMON.PROC.BU.1#3:
PASS
[PASS] Max = 325ms. Obtained time difference is 39.04ms
Packet 131
Rev3ChkdSnk:
PASS
Response Check - TEST.PD.PROT.ALL3.4#2:
PASS
DUT sent Manufacturer_Info message for the Get_Manufacturer_Info
Manufacturer String Check - TEST.PD.PROT.ALL3.4#3:

PASS

DUT manufacture info string matched with specified format Rev3UnchkdSnk:

PASS

Response Check - TEST.PD.PROT.ALL3.4#2:

PASS

DUT sent Manufacturer_Info message for the Get_Manufacturer_Info

Manufacturer String Check - TEST.PD.PROT.ALL3.4#3:

PASS

DUT manufacture info string matched with specified format Rev3ChkdSrc:

PASS

Response Check - TEST.PD.PROT.ALL3.4#2:

PASS

DUT sent Manufacturer_Info message for the Get_Manufacturer_Info

Manufacturer String Check - TEST.PD.PROT.ALL3.4#3:

PASS

DUT manufacture info string matched with specified format Rev3UnchkdSrc:

PASS

Response Check - TEST.PD.PROT.ALL3.4#2:

PASS

DUT sent Manufacturer_Info message for the Get_Manufacturer_Info

Manufacturer String Check - TEST.PD.PROT.ALL3.4#3:

PASS

DUT manufacture info string matched with specified format

20. TEST.PD.PROT.ALL3.5 Chunked Extended Message Response (Click

PASS to View Protocol Trace)

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet16

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet18

Rev3ChkdSnk:

PASS

Chunk Response - TEST.PD.PROT.ALL3.5#2:

PASS

[PASS] UUT sent request for Data block Obtained time difference is 4.218ms, Expected time limit 0ms to 15ms

Chunk message field check - TEST.PD.PROT.ALL3.5#3:

PASS

Requested chunk message response - TEST.PD.PROT.ALL3.5#4:

PASS

DUT responded with Not_Supported message for Reserved message. Actual time interval is: 4.139ms

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 4.562s and SourceCap time: 4.744s at protocol index #93

[PASS] Max = 250ms. Obtained time difference is 181.649ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet97

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.493ms

Packet 99

Rev3ChkdSrc:

PASS

Chunk Response - TEST.PD.PROT.ALL3.5#2:

PASS

[PASS] UUT sent request for Data block Obtained time difference is 2.787ms, Expected time limit 0ms to 15ms

Chunk message field check - TEST.PD.PROT.ALL3.5#3:

PASS

Requested chunk message response - TEST.PD.PROT.ALL3.5#4:

PASS

DUT responded with Not_Supported message for Reserved message. Actual time interval is: 4.139ms

21. TEST.PD.PROT.ALL3.6 ChunkSenderResponseTimer Timeout (Click

PASS to View Protocol Trace)

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet15

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet17

Rev3ChkdSnk:

PASS

Chunk Response - TEST.PD.PROT.ALL3.6#2:

PASS

UUT respond with Reserved message for the Tester initiated Chunk extended message at protocol index: 33

[PASS] UUT sent request for Data block Obtained time difference is 5.068ms, Expected time limit 0ms to 15ms

Chunk message field check - TEST.PD.PROT.ALL3.6#3:

PASS

DUT responded with Reserved message for Reserved message. Actual time interval is: 0.643ms

Response Check - TEST.PD.PROT.ALL3.6#5:

PASS

DUT responded with Reserved message for Reserved message.
Actual time interval is: 9.457ms

Message Header and Extended Message Header -
PASS TEST.PD.PROT.ALL3.6#6:

COMMON.PROC.BU.1:
PASS

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:
PASS

First source capability timer - COMMON.PROC.BU.1#1:
PASS

Vbus up time: 4.452s and SourceCap time: 4.64s at protocol index #112
[PASS] Max = 250ms. Obtained time difference is 187.481ms

DUT responded with accept message - COMMON.PROC.BU.1#2:
PASS

Packet116

tSrcTransReq timer check - COMMON.PROC.BU.1#3:
PASS

[PASS] Max = 325ms. Obtained time difference is 40.101ms
Packet 118

Rev3ChkdSrc:
PASS

Chunk Response - TEST.PD.PROT.ALL3.6#2:
PASS

UUT respond with Reserved message for the Tester initiated Chunk extended message at protocol index: 126
[PASS] UUT sent request for Data block Obtained time difference is 3.538ms, Expected time limit 0ms to 15ms

Chunk message field check - TEST.PD.PROT.ALL3.6#3:
PASS

DUT responded with Reserved message for Reserved message.
Actual time interval is: 0.643ms

Response Check - TEST.PD.PROT.ALL3.6#5:
PASS

DUT responded with Reserved message for Reserved message.
Actual time interval is: 9.457ms

Message Header and Extended Message Header -
PASS TEST.PD.PROT.ALL3.6#6:

22. TEST.PD.PROT.ALL3.7 Security Messages Supported (Click to View
PASS Protocol Trace)

COMMON.PROC.BU.2:
PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:
PASS

SourceCap Packet15

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet17

COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk:
PASS

SourceCap Packet55

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet57

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 8.411s and SourceCap time: 8.593s at protocol index #96

[PASS] Max = 250ms. Obtained time difference is 182.482ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet100

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.248ms

Packet 102

COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 11.517s and SourceCap time: 11.701s at protocol index #127

[PASS] Max = 250ms. Obtained time difference is 184.148ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet131

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.458ms

Packet 133

Rev3ChkdSnk:

PASS

Security Request message response check - TEST.PD.PROT.ALL3.7#1:

PASS

VIF field Security_Msgs_Supported_SOP is No. and UUT respond with Not_Supported message at protocol index 33

Rev3UnchkdSnk:

PASS

Security Request message response check - TEST.PD.PROT.ALL3.7#1:

PASS

VIF field Security_Msgs_Supported_SOP is No. and UUT respond with Not_Supported message at protocol index 73

Rev3ChkdSrc:

PASS

Security Request message response check - TEST.PD.PROT.ALL3.7#1:

PASS

VIF field Security_Msgs_Supported_SOP is No. and UUT respond with Not_Supported message at protocol index 110

Rev3UnchkdSrc:

PASS

Security Request message response check - TEST.PD.PROT.ALL3.7#1:
PASS

VIF field Security_Msgs_Supported_SOP is No. and UUT respond with Not_Supported message at protocol index 141

23. TEST.PD.PROT.ALL3.8 Get Revision Response (Click to View Protocol Trace)
PASS

COMMON.PROC.BU.2:
PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:
PASS

SourceCap Packet15

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet17

Rev3ChkdSnk:
PASS

Get_Revision response check - TEST.PD.PROT.ALL3.8#1:
PASS

UUT responded with Revision message for Tester's Get_Revision message

Revision message details check - TEST.PD.PROT.ALL3.8#2:
PASS

UUT responded Revision message for Tester's Get_Revision The Number of Data objects in Revision message header is 1

Revision_Major field with respect to VIF file, DUT sent 3 to VIF field 3

Revison_Minor field with respect to VIF file, DUT sent 1 to VIF field 1

Version_Major field with respect to VIF file, DUT sent 1 to VIF field 1

Version_Minor field with respect to VIF file, DUT sent 8 to VIF field 8

COMMON.PROC.BU.1:
PASS

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:
PASS

First source capability timer - COMMON.PROC.BU.1#1:
PASS

Vbus up time: 4.203s and SourceCap time: 4.385s at protocol index #55

[PASS] Max = 250ms. Obtained time difference is 182.482ms

DUT responded with accept message - COMMON.PROC.BU.1#2:
PASS

Packet59

tSrcTransReq timer check - COMMON.PROC.BU.1#3:
PASS

[PASS] Max = 325ms. Obtained time difference is 41.076ms

Packet 61

Rev3ChkdSrc:
PASS

Get_Revision response check - TEST.PD.PROT.ALL3.8#1:
PASS

UUT responded with Revision message for Tester's Get_Revision message

Revision message details check - TEST.PD.PROT.ALL3.8#2:

PASS

UUT responded Revision message for Tester's Get_Revision The Number of Data objects in Revision message header is 1

Revision_Major field with respect to VIF file, DUT sent 3 to VIF field 3

Revison_Minor field with respect to VIF file, DUT sent 1 to VIF field 1

Version_Major field with respect to VIF file, DUT sent 1 to VIF field 1

Version_Minor field with respect to VIF file, DUT sent 8 to VIF field 8

24. TEST.PD.PROT.PORT3.1 Get Battery Status Response (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet15

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet17

Rev3ChkdSnk:

PASS

Get_Sink_Cap_Ext response check - TEST.PD.PROT.PORT3.1#1:

PASS

UUT responded with Sink_Cap_Extended to Get_Sink_Cap_Ext message at protocol index 33.

Get_Battery_Status response check - TEST.PD.PROT.PORT3.1#2:

PASS

UUT respond Battery_Status PD Message.Packet43
UUT respond Battery_Status PD Message.Packet48
UUT respond Battery_Status PD Message.Packet53
UUT respond Battery_Status PD Message.Packet58
UUT respond Battery_Status PD Message.Packet63
UUT respond Battery_Status PD Message.Packet68
UUT respond Battery_Status PD Message.Packet73
UUT respond Battery_Status PD Message.Packet78

Battery_Status message check - TEST.PD.PROT.PORT3.1#4:

PASS

[PASS]Battery Info Field : BSDO bits zero
[PASS]Battery Info Field : Reserved bits zero
UUT responded with Sink_Cap_Extended to Get_Sink_Cap_Ext message.
[PASS]The values of VIF fields Num_Fixed_Batteries(Expected) : 1, Fixed_Batteries(Obtained) : 1
Num_Swappable_Battery_Slots(Expected) : 0, Hot_Swap_Batteries(Obtained) : 0
[PASS]In BSDO Invalid Battery Reference bit[0] is 0.Battery present bit[1] is 1.In GBSDB Battery status ref field is 0
[PASS]In BSDO Battery present bit[1] is 1.Battery charging status bit[3:2] is 0

[PASS]Battery Info Field : BSDO bits zero
[PASS]Battery Info Field : Reserved bits zero
UUT responded with Sink_Cap_Extended to Get_Sink_Cap_Ext message.
[PASS]The values of VIF fields Num_Fixed_Batteries(Expected) : 1, Fixed_Batteries(Obtained) : 1
Num_Swappable_Battery_Slots(Expected) : 0, Hot_Swap_Batteries(Obtained) : 0
[PASS]In BSDO Invalid Battery Reference bit[0] is 1.Battery present bit[1] is 0.Battery charging status bit[3:2] is 0
[PASS]In BSDO Battery present bit[1] is 0.Battery charging status bit[3:2] is 0
[PASS]Battery Info Field : BSDO bits zero
[PASS]Battery Info Field : Reserved bits zero
UUT responded with Sink_Cap_Extended to Get_Sink_Cap_Ext message.
[PASS]The values of VIF fields Num_Fixed_Batteries(Expected) : 1, Fixed_Batteries(Obtained) : 1
Num_Swappable_Battery_Slots(Expected) : 0, Hot_Swap_Batteries(Obtained) : 0
[PASS]In BSDO Invalid Battery Reference bit[0] is 1.Battery present bit[1] is 0.Battery charging status bit[3:2] is 0
[PASS]In BSDO Battery present bit[1] is 0.Battery charging status bit[3:2] is 0
[PASS]Battery Info Field : BSDO bits zero
[PASS]Battery Info Field : Reserved bits zero
UUT responded with Sink_Cap_Extended to Get_Sink_Cap_Ext message.
[PASS]The values of VIF fields Num_Fixed_Batteries(Expected) : 1, Fixed_Batteries(Obtained) : 1
Num_Swappable_Battery_Slots(Expected) : 0, Hot_Swap_Batteries(Obtained) : 0
[PASS]In BSDO Invalid Battery Reference bit[0] is 1.Battery present bit[1] is 0.Battery charging status bit[3:2] is 0
[PASS]In BSDO Battery present bit[1] is 0.Battery charging status bit[3:2] is 0
[PASS]Battery Info Field : BSDO bits zero
[PASS]Battery Info Field : Reserved bits zero
UUT responded with Sink_Cap_Extended to Get_Sink_Cap_Ext message.
[PASS]The values of VIF fields Num_Fixed_Batteries(Expected) : 1, Fixed_Batteries(Obtained) : 1
Num_Swappable_Battery_Slots(Expected) : 0, Hot_Swap_Batteries(Obtained) : 0
[PASS]In BSDO Invalid Battery Reference bit[0] is 1.Battery present bit[1] is 0.Battery charging status bit[3:2] is 0
[PASS]In BSDO Battery present bit[1] is 0.Battery charging status bit[3:2] is 0
[PASS]Battery Info Field : BSDO bits zero
[PASS]Battery Info Field : Reserved bits zero
UUT responded with Sink_Cap_Extended to Get_Sink_Cap_Ext message.
[PASS]The values of VIF fields Num_Fixed_Batteries(Expected) : 1, Fixed_Batteries(Obtained) : 1
Num_Swappable_Battery_Slots(Expected) : 0, Hot_Swap_Batteries(Obtained) : 0
[PASS]In BSDO Invalid Battery Reference bit[0] is 1.Battery present bit[1] is 0.Battery charging status bit[3:2] is 0

[PASS]In BSDO Battery present bit[1] is 0.Battery charging status bit[3:2] is 0
[PASS]Battery Info Field : BSDO bits zero
[PASS]Battery Info Field : Reserved bits zero
UUT responded with Sink_Cap_Extended to Get_Sink_Cap_Ext message.
[PASS]The values of VIF fields Num_Fixed_Batteries(Expected) : 1, Fixed_Batteries(Obtained) : 1
Num_Swappable_Battery_Slots(Expected) : 0, Hot_Swap_Batteries(Obtained) : 0
[PASS]In BSDO Invalid Battery Reference bit[0] is 1.Battery present bit[1] is 0.Battery charging status bit[3:2] is 0
[PASS]In BSDO Battery present bit[1] is 0.Battery charging status bit[3:2] is 0
[PASS]Battery Info Field : BSDO bits zero
[PASS]Battery Info Field : Reserved bits zero
UUT responded with Sink_Cap_Extended to Get_Sink_Cap_Ext message.
[PASS]The values of VIF fields Num_Fixed_Batteries(Expected) : 1, Fixed_Batteries(Obtained) : 1
Num_Swappable_Battery_Slots(Expected) : 0, Hot_Swap_Batteries(Obtained) : 0
[PASS]In BSDO Invalid Battery Reference bit[0] is 1.Battery present bit[1] is 0.Battery charging status bit[3:2] is 0
[PASS]In BSDO Battery present bit[1] is 0.Battery charging status bit[3:2] is 0

COMMON.PROC.BU.1:
PASS

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:
PASS

First source capability timer - COMMON.PROC.BU.1#1:
PASS

Vbus up time: 4.296s and SourceCap time: 4.482s at protocol index #96
[PASS] Max = 250ms. Obtained time difference is 185.815ms

DUT responded with accept message - COMMON.PROC.BU.1#2:
PASS

Packet100

tSrcTransReq timer check - COMMON.PROC.BU.1#3:
PASS

[PASS] Max = 325ms. Obtained time difference is 41.114ms
Packet 102

Rev3ChkdSrc:
PASS

Get_SourceCap_Extended response check - TEST.PD.PROT.PORT3.1#1:
PASS

UUT responded with Source_Cap_Extended to Get_SourceCap_Extended message at protocol index 110.

Get_Battery_Status response check - TEST.PD.PROT.PORT3.1#2:
PASS

UUT respond Battery_Status PD Message.Packet115
UUT respond Battery_Status PD Message.Packet120
UUT respond Battery_Status PD Message.Packet125
UUT respond Battery_Status PD Message.Packet130

UUT respond Battery_Status PD Message.Packet135
UUT respond Battery_Status PD Message.Packet140
UUT respond Battery_Status PD Message.Packet145
UUT respond Battery_Status PD Message.Packet150
Battery_Status message check - TEST.PD.PROT.PORT3.1#4:
PASS
[PASS]Battery Info Field : BSDO bits zero
[PASS]Battery Info Field : Reserved bits zero
UUT responded with Source_Cap_Extended to Get_SourceCap_Extended message.
[PASS]The values of VIF fields Num_Fixed_Batteries(Expected) : 1, Fixed_Batteries(Obtained) : 1
Num_Swappable_Battery_Slots(Expected) : 0, Hot_Swap_Batteries(Obtained) : 0
[PASS]In BSDO Invalid Battery Reference bit[0] is 0.Battery present bit[1] is 1.In GBSDB Battery status ref field is 0
[PASS]In BSDO Battery present bit[1] is 1.Battery charging status bit[3:2] is 0
[PASS]Battery Info Field : BSDO bits zero
[PASS]Battery Info Field : Reserved bits zero
UUT responded with Source_Cap_Extended to Get_SourceCap_Extended message.
[PASS]The values of VIF fields Num_Fixed_Batteries(Expected) : 1, Fixed_Batteries(Obtained) : 1
Num_Swappable_Battery_Slots(Expected) : 0, Hot_Swap_Batteries(Obtained) : 0
[PASS]In BSDO Invalid Battery Reference bit[0] is 1.Battery present bit[1] is 0.Battery charging status bit[3:2] is 0
[PASS]In BSDO Battery present bit[1] is 0.Battery charging status bit[3:2] is 0
[PASS]Battery Info Field : BSDO bits zero
[PASS]Battery Info Field : Reserved bits zero
UUT responded with Source_Cap_Extended to Get_SourceCap_Extended message.
[PASS]The values of VIF fields Num_Fixed_Batteries(Expected) : 1, Fixed_Batteries(Obtained) : 1
Num_Swappable_Battery_Slots(Expected) : 0, Hot_Swap_Batteries(Obtained) : 0
[PASS]In BSDO Invalid Battery Reference bit[0] is 1.Battery present bit[1] is 0.Battery charging status bit[3:2] is 0
[PASS]In BSDO Battery present bit[1] is 0.Battery charging status bit[3:2] is 0
[PASS]Battery Info Field : BSDO bits zero
[PASS]Battery Info Field : Reserved bits zero
UUT responded with Source_Cap_Extended to Get_SourceCap_Extended message.
[PASS]The values of VIF fields Num_Fixed_Batteries(Expected) : 1, Fixed_Batteries(Obtained) : 1
Num_Swappable_Battery_Slots(Expected) : 0, Hot_Swap_Batteries(Obtained) : 0
[PASS]In BSDO Invalid Battery Reference bit[0] is 1.Battery present bit[1] is 0.Battery charging status bit[3:2] is 0
[PASS]In BSDO Battery present bit[1] is 0.Battery charging status bit[3:2] is 0
[PASS]Battery Info Field : BSDO bits zero
[PASS]Battery Info Field : Reserved bits zero
UUT responded with Source_Cap_Extended to

Get_SourceCap_Extended message.

[PASS]The values of VIF fields Num_Fixed_Batteries(Expected) : 1, Fixed_Batteries(Obtained) : 1

Num_Swappable_Battery_Slots(Expected) : 0, Hot_Swap_Batteries(Obtained) : 0

[PASS]In BSDO Invalid Battery Reference bit[0] is 1.Battery present bit[1] is 0.Battery charging status bit[3:2] is 0

[PASS]In BSDO Battery present bit[1] is 0.Battery charging status bit[3:2] is 0

[PASS]Battery Info Field : BSDO bits zero

[PASS]Battery Info Field : Reserved bits zero

UUT responded with Source_Cap_Extended to Get_SourceCap_Extended message.

[PASS]The values of VIF fields Num_Fixed_Batteries(Expected) : 1, Fixed_Batteries(Obtained) : 1

Num_Swappable_Battery_Slots(Expected) : 0, Hot_Swap_Batteries(Obtained) : 0

[PASS]In BSDO Invalid Battery Reference bit[0] is 1.Battery present bit[1] is 0.Battery charging status bit[3:2] is 0

[PASS]In BSDO Battery present bit[1] is 0.Battery charging status bit[3:2] is 0

[PASS]Battery Info Field : BSDO bits zero

[PASS]Battery Info Field : Reserved bits zero

UUT responded with Source_Cap_Extended to Get_SourceCap_Extended message.

[PASS]The values of VIF fields Num_Fixed_Batteries(Expected) : 1, Fixed_Batteries(Obtained) : 1

Num_Swappable_Battery_Slots(Expected) : 0, Hot_Swap_Batteries(Obtained) : 0

[PASS]In BSDO Invalid Battery Reference bit[0] is 1.Battery present bit[1] is 0.Battery charging status bit[3:2] is 0

[PASS]In BSDO Battery present bit[1] is 0.Battery charging status bit[3:2] is 0

[PASS]Battery Info Field : BSDO bits zero

[PASS]Battery Info Field : Reserved bits zero

UUT responded with Source_Cap_Extended to Get_SourceCap_Extended message.

[PASS]The values of VIF fields Num_Fixed_Batteries(Expected) : 1, Fixed_Batteries(Obtained) : 1

Num_Swappable_Battery_Slots(Expected) : 0, Hot_Swap_Batteries(Obtained) : 0

[PASS]In BSDO Invalid Battery Reference bit[0] is 1.Battery present bit[1] is 0.Battery charging status bit[3:2] is 0

[PASS]In BSDO Battery present bit[1] is 0.Battery charging status bit[3:2] is 0

PASS 25. TEST.PD.PROT.PORT3.2 Invalid Battery Status (Click to View Protocol Trace)

PASS COMMON.PROC.BU.2:

PASS COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

SourceCap Packet15

PASS UUT should respond with request - - COMMON.PROC.BU.2#1:

Request Packet17

Rev3ChkdSnk:

PASS

Get_Sink_Cap_Ext response check - TEST.PD.PROT.PORT3.2#1:

PASS

UUT responded with Sink_Cap_Extended to Get_Sink_Cap_Ext message at protocol index 33.

Battery_Status message check - TEST.PD.PROT.PORT3.2#4:

PASS

Battery Info Field : BSDO bits are zero
In Battery_Status message Invalid_Battery_Ref field is correct.
Battery_Info field is correct from 1 to 7 bits.

Get_Battery_Status response check - TEST.PD.PROT.PORT3.2#2:

PASS

UUT respond Battery_Status to Get_Battery_Status message

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 4.531s and SourceCap time: 4.711s at protocol index #65

[PASS] Max = 250ms. Obtained time difference is 179.982ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet69

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 41.09ms
Packet 71

Rev3ChkdSrc:

PASS

Get_SourceCap_Extended response check -

PASS TEST.PD.PROT.PORT3.2#1:

UUT responded with Source_Cap_Extended to Get_SourceCap_Extended message at protocol index 79.

Battery_Status message check - TEST.PD.PROT.PORT3.2#4:

PASS

Battery Info Field : BSDO bits are zero
In Battery_Status message Invalid_Battery_Ref field is correct.
Battery_Info field is correct from 1 to 7 bits.

Get_Battery_Status response check - TEST.PD.PROT.PORT3.2#2:

PASS

UUT respond Battery_Status to Get_Battery_Status message

26. TEST.PD.PROT.PORT3.3 Get Battery Cap Response (Click to View

PASS Protocol Trace)

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet15

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet17
COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk:
PASS
SourceCap Packet134
UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS
Request Packet136
COMMON.PROC.BU.1:
PASS
COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:
PASS
First source capability timer - COMMON.PROC.BU.1#1:
PASS
Vbus up time: 12.214s and SourceCap time: 12.396s at protocol index #254
[PASS] Max = 250ms. Obtained time difference is 181.649ms
DUT responded with accept message - COMMON.PROC.BU.1#2:
PASS
Packet258
tSrcTransReq timer check - COMMON.PROC.BU.1#3:
PASS
[PASS] Max = 325ms. Obtained time difference is 39.725ms
Packet 260
COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc:
PASS
First source capability timer - COMMON.PROC.BU.1#1:
PASS
Vbus up time: 17.176s and SourceCap time: 17.365s at protocol index #325
[PASS] Max = 250ms. Obtained time difference is 189.148ms
DUT responded with accept message - COMMON.PROC.BU.1#2:
PASS
Packet329
tSrcTransReq timer check - COMMON.PROC.BU.1#3:
PASS
[PASS] Max = 325ms. Obtained time difference is 39.559ms
Packet 331
Rev3ChkdSnk:
PASS
Get_Sink_Cap_Ext check - TEST.PD.PROT.PORT3.3#1:
PASS
UUT responded with Sink_Cap_Extended to Get_Sink_Cap_Ext message at protocol index 33.
Get_Battery_Cap check - TEST.PD.PROT.PORT3.3#2:
PASS
Get_Battery_Cap check for Battery_Cap_Ref_#0 -
PASS TEST.PD.PROT.PORT3.3#2:
UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0
Get_Battery_Cap check for Battery_Cap_Ref_#1 -

PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#2 -
PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#3 -
PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#4 -
PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#5 -
PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#6 -
PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#7 -
PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Battery_Capabilities check - TEST.PD.PROT.PORT3.3#3:
PASS

Battery_Capabilities check for Battery_Cap_Ref_#0 -
PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 0 at protocol index 43
Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#1 -
PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 53
Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#2 -
PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 63
Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#3 -
PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 73

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#4 - PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 83

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#5 - PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 93

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#6 - PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 103

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#7 - PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 113

Battery type bit[1..7] is zero

Rev3UnchkdSnk:

PASS

Get_Sink_Cap_Ext check - TEST.PD.PROT.PORT3.3#1:

PASS

UUT responded with Sink_Cap_Extended to Get_Sink_Cap_Ext message at protocol index 152.

Get_Battery_Cap check - TEST.PD.PROT.PORT3.3#2:

PASS

Get_Battery_Cap check for Battery_Cap_Ref_#0 - PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message

The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#1 - PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message

The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#2 - PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message

The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#3 - PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message

The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#4 - PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#5 - PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#6 - PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#7 - PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Battery_Capabilities check - TEST.PD.PROT.PORT3.3#3: PASS

Battery_Capabilities check for Battery_Cap_Ref_#0 - PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 0 at protocol index 162

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#1 - PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 172

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#2 - PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 182

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#3 - PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 192

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#4 - PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 202

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#5 - PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 212

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#6 - PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol

index 222

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#7 -
PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 232

Battery type bit[1..7] is zero

Rev3ChkdSrc:
PASS

Get_SourceCap_Extended check - TEST.PD.PROT.PORT3.3#1:
PASS

UUT responded with Source_Cap_Extended to Get_SourceCap_Extended message at protocol index 268.

Get_Battery_Cap check - TEST.PD.PROT.PORT3.3#2:
PASS

Get_Battery_Cap check for Battery_Cap_Ref_#0 -
PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#1 -
PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#2 -
PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#3 -
PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#4 -
PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#5 -
PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#6 -
PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#7 -
PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message

The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Battery_Capabilities check - TEST.PD.PROT.PORT3.3#3:

PASS

Battery_Capabilities check for Battery_Cap_Ref_#0 -

PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 0 at protocol index 273

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#1 -

PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 278

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#2 -

PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 283

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#3 -

PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 288

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#4 -

PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 293

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#5 -

PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 298

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#6 -

PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 303

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#7 -

PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 308

Battery type bit[1..7] is zero

Rev3UnchkdSrc:

PASS

Get_SourceCap_Extended check - TEST.PD.PROT.PORT3.3#1:

PASS

UUT responded with Source_Cap_Extended to Get_SourceCap_Extended message at protocol index 339.

Get_Battery_Cap check - TEST.PD.PROT.PORT3.3#2:

PASS

Get_Battery_Cap check for Battery_Cap_Ref_#0 -
PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#1 -
PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#2 -
PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#3 -
PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#4 -
PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#5 -
PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#6 -
PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Get_Battery_Cap check for Battery_Cap_Ref_#7 -
PASS TEST.PD.PROT.PORT3.3#2:

UUT respond Battery_Capabilities to Get_Battery_Cap message
The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0

Battery_Capabilities check - TEST.PD.PROT.PORT3.3#3:
PASS

Battery_Capabilities check for Battery_Cap_Ref_#0 -
PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 0 at protocol index 344

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#1 -
PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 349

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#2 -

PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 354

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#3 -

PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 359

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#4 -

PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 364

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#5 -

PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 369

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#6 -

PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 374

Battery type bit[1..7] is zero

Battery_Capabilities check for Battery_Cap_Ref_#7 -

PASS TEST.PD.PROT.PORT3.3#3:

Obtained Invalid Battery Reference field value: 1 at protocol index 379

Battery type bit[1..7] is zero

27. TEST.PD.PROT.PORT3.4 Invalid Battery Capabilities Reference

PASS (Click to View Protocol Trace)

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet15

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet17

COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk:

PASS

SourceCap Packet64

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet66

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 7.918s and SourceCap time: 8.102s at protocol

index #114

[PASS] Max = 250ms. Obtained time difference is 183.315ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet118

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.791ms

Packet 120

COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 10.763s and SourceCap time: 10.949s at protocol index #150

[PASS] Max = 250ms. Obtained time difference is 185.815ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet154

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.776ms

Packet 156

Rev3ChkdSnk:

PASS

Get_Sink_Cap_Ext check - TEST.PD.PROT.PORT3.4#1:

PASS

UUT responded with Sink_Cap_Extended to Get_Sink_Cap_Ext message at protocol index 33.

Get_Battery_Cap check - TEST.PD.PROT.PORT3.4#2:

PASS

UUT respond Battery_Capabilities to Get_Battery_Cap message

Battery_Capabilities check - TEST.PD.PROT.PORT3.4#3:

PASS

[Bit 0]:Invalid battery reference field is 1

[Bit 1..7]:Battery type bit is 0

Rev3UnchkdSnk:

PASS

Get_Sink_Cap_Ext check - TEST.PD.PROT.PORT3.4#1:

PASS

UUT responded with Sink_Cap_Extended to Get_Sink_Cap_Ext message at protocol index 82.

Get_Battery_Cap check - TEST.PD.PROT.PORT3.4#2:

PASS

UUT respond Battery_Capabilities to Get_Battery_Cap message

Battery_Capabilities check - TEST.PD.PROT.PORT3.4#3:

PASS

[Bit 0]:Invalid battery reference field is 1

[Bit 1..7]:Battery type bit is 0

Rev3ChkdSrc:

PASS

Get_SourceCap_Extended check - TEST.PD.PROT.PORT3.4#1:

PASS

UUT responded with Source_Cap_Extended to Get_SourceCap_Extended message at protocol index 128.

Get_Battery_Cap check - TEST.PD.PROT.PORT3.4#2:

PASS

UUT respond Battery_Capabilities to Get_Battery_Cap message

Battery_Capabilities check - TEST.PD.PROT.PORT3.4#3:

PASS

[Bit 0]:Invalid battery reference field is 1

[Bit 1..7]:Battery type bit is 0

Rev3UnchkdSrc:

PASS

Get_SourceCap_Extended check - TEST.PD.PROT.PORT3.4#1:

PASS

UUT responded with Source_Cap_Extended to Get_SourceCap_Extended message at protocol index 164.

Get_Battery_Cap check - TEST.PD.PROT.PORT3.4#2:

PASS

UUT respond Battery_Capabilities to Get_Battery_Cap message

Battery_Capabilities check - TEST.PD.PROT.PORT3.4#3:

PASS

[Bit 0]:Invalid battery reference field is 1

[Bit 1..7]:Battery type bit is 0

28. TEST.PD.PROT.PORT3.5 Get Country Codes Response (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet16

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet18

COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk:

PASS

SourceCap Packet65

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet67

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 7.798s and SourceCap time: 7.983s at protocol index #115

[PASS] Max = 250ms. Obtained time difference is 184.982ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet119

tSrcTransReq timer check - COMMON.PROC.BU.1#3:
PASS

[PASS] Max = 325ms. Obtained time difference is 40.099ms
Packet 121

COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc:
PASS

First source capability timer - COMMON.PROC.BU.1#1:
PASS

Vbus up time: 10.606s and SourceCap time: 10.791s at protocol index #154

[PASS] Max = 250ms. Obtained time difference is 184.981ms

DUT responded with accept message - COMMON.PROC.BU.1#2:
PASS

Packet158

tSrcTransReq timer check - COMMON.PROC.BU.1#3:
PASS

[PASS] Max = 325ms. Obtained time difference is 40.649ms
Packet 160

Rev3ChkdSnk:
PASS

Country Code Data Block(CCDB) check - TEST.PD.PROT.PORT3.5#2:
PASS

Country code length matched with Datasize.

Country_Codes check - TEST.PD.PROT.PORT3.5#1:
PASS

UUT respond Country_Codes message to Get_Country_Codes message

Rev3UnchkdSnk:
PASS

Country Code Data Block(CCDB) check - TEST.PD.PROT.PORT3.5#2:
PASS

Country code length matched with Datasize.

Country_Codes check - TEST.PD.PROT.PORT3.5#1:
PASS

UUT respond Country_Codes message to Get_Country_Codes message

Rev3ChkdSrc:
PASS

Country Code Data Block(CCDB) check - TEST.PD.PROT.PORT3.5#2:
PASS

Country code length matched with Datasize.

Country_Codes check - TEST.PD.PROT.PORT3.5#1:
PASS

UUT respond Country_Codes message to Get_Country_Codes message

Rev3UnchkdSrc:
PASS

Country Code Data Block(CCDB) check - TEST.PD.PROT.PORT3.5#2:
PASS

Country code length matched with Datasize.

Country_Codes check - TEST.PD.PROT.PORT3.5#1:
PASS

UUT respond Country_Codes message to Get_Country_Codes message

29. TEST.PD.PROT.PORT3.6 Get Country Info Response (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet15

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet17

COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk:

PASS

SourceCap Packet64

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet66

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 7.804s and SourceCap time: 7.988s at protocol index #114

[PASS] Max = 250ms. Obtained time difference is 183.315ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet118

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.61ms

Packet 120

COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 10.61s and SourceCap time: 10.796s at protocol index #153

[PASS] Max = 250ms. Obtained time difference is 185.815ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet157

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.65ms

Packet 159

Rev3ChkdSnk:

PASS

Country_Codes check - TEST.PD.PROT.PORT3.6#1:

PASS

UUT respond Country_Codes message to Get_Country_Codes message

Country_Info check - TEST.PD.PROT.PORT3.6#2:

PASS

UUT respond Country_Info to Get_Country_Info message

UUT respond Country_Info to Get_Country_Info message

Country Info Data Block(CIDB) check - TEST.PD.PROT.PORT3.6#3:

PASS

Country code of Country_Info first character is matched with Get_Country_Info first character.

Country code of Country_Info second character is matched with Get_Country_Info second character.

Country_Info byte2 is zero.

Country_Info byte3 is zero.

Country code of Country_Info first character is matched with Get_Country_Info first character.

Country code of Country_Info second character is matched with Get_Country_Info second character.

Country_Info byte2 is zero.

Country_Info byte3 is zero.

Rev3UnchkdSnk:

PASS

Country_Codes check - TEST.PD.PROT.PORT3.6#1:

PASS

UUT respond Country_Codes message to Get_Country_Codes message

Country_Info check - TEST.PD.PROT.PORT3.6#2:

PASS

UUT respond Country_Info to Get_Country_Info message

UUT respond Country_Info to Get_Country_Info message

Country Info Data Block(CIDB) check - TEST.PD.PROT.PORT3.6#3:

PASS

Country code of Country_Info first character is matched with Get_Country_Info first character.

Country code of Country_Info second character is matched with Get_Country_Info second character.

Country_Info byte2 is zero.

Country_Info byte3 is zero.

Country code of Country_Info first character is matched with Get_Country_Info first character.

Country code of Country_Info second character is matched with Get_Country_Info second character.

Country_Info byte2 is zero.

Country_Info byte3 is zero.

Rev3ChkdSrc:

PASS

Country_Codes check - TEST.PD.PROT.PORT3.6#1:

PASS

UUT respond Country_Codes message to Get_Country_Codes message

Country_Info check - TEST.PD.PROT.PORT3.6#2:

PASS

UUT respond Country_Info to Get_Country_Info message

UUT respond Country_Info to Get_Country_Info message

Country Info Data Block(CIDB) check - TEST.PD.PROT.PORT3.6#3:

PASS

Country code of Country_Info first character is matched with Get_Country_Info first character.

Country code of Country_Info second character is matched with Get_Country_Info second character.

Country_Info byte2 is zero.

Country_Info byte3 is zero.

Country code of Country_Info first character is matched with Get_Country_Info first character.

Country code of Country_Info second character is matched with Get_Country_Info second character.

Country_Info byte2 is zero.

Country_Info byte3 is zero.

Rev3UnchkdSrc:

PASS

Country_Codes check - TEST.PD.PROT.PORT3.6#1:

PASS

UUT respond Country_Codes message to Get_Country_Codes message

Country_Info check - TEST.PD.PROT.PORT3.6#2:

PASS

UUT respond Country_Info to Get_Country_Info message

UUT respond Country_Info to Get_Country_Info message

Country Info Data Block(CIDB) check - TEST.PD.PROT.PORT3.6#3:

PASS

Country code of Country_Info first character is matched with Get_Country_Info first character.

Country code of Country_Info second character is matched with Get_Country_Info second character.

Country_Info byte2 is zero.

Country_Info byte3 is zero.

Country code of Country_Info first character is matched with Get_Country_Info first character.

Country code of Country_Info second character is matched with Get_Country_Info second character.

Country_Info byte2 is zero.

Country_Info byte3 is zero.

NA **30. TEST.PD.PROT.PORT3.7 Unchunked Extended Message Supported** (Click to View Protocol Trace)

In VIF Unchunked_Extended_Messages_Supported field is NO

31. TEST.PD.PROT.SRC.1 Get_Source_Cap Response (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 1.13s and SourceCap time: 1.314s at protocol index #16

[PASS] Max = 250ms. Obtained time difference is 184.148ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.232ms

Packet 22

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 4.232s and SourceCap time: 4.418s at protocol index #53

[PASS] Max = 250ms. Obtained time difference is 185.815ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet57

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.703ms

Packet 59

Rev2Src:

PASS

Source_Cap message check - TEST.PD.PROT.SRC.1#1:

PASS

UUT is successfully respond to Get_Source_Cap message.Protocol index #30

Rev3ChkdSrc:

PASS

Source_Cap message check - TEST.PD.PROT.SRC.1#1:

PASS

UUT is successfully respond to Get_Source_Cap message.Protocol index #67

32. TEST.PD.PROT.SRC.2 Get_Source_Cap No Request (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 1.13s and SourceCap time: 1.317s at protocol index #16

[PASS] Max = 250ms. Obtained time difference is 187.481ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.044ms

Packet 22

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:
PASS

Vbus up time: 5.64s and SourceCap time: 5.825s at protocol index #62

[PASS] Max = 250ms. Obtained time difference is 184.981ms

DUT responded with accept message - COMMON.PROC.BU.1#2:
PASS

Packet66

tSrcTransReq timer check - COMMON.PROC.BU.1#3:
PASS

[PASS] Max = 325ms. Obtained time difference is 40.122ms

Packet 68

Rev2Src:
PASS

Source_Cap message check - TEST.PD.PROT.SRC.2#1:
PASS

UUT successfully respond to Get_Source_Cap message.Protocol index #30

Hard_Reset message check - TEST.PD.PROT.SRC.2#2:
PASS

UUT responded with Hard_Reset within 0.024~0.03s.Obtained interval is 0.02576s.Protocol index #32

Rev3ChkdSrc:
PASS

Source_Cap message check - TEST.PD.PROT.SRC.2#1:
PASS

UUT successfully respond to Get_Source_Cap message.Protocol index #76

Hard_Reset message check - TEST.PD.PROT.SRC.2#2:
PASS

UUT responded with Hard_Reset within 0.027~0.033s.Obtained interval is 0.0277s.Protocol index #78

33. TEST.PD.PROT.SRC.3 Sender Response Timer Deadline (Click to View Protocol Trace)
PASS

Rev2Src:
PASS

tFirstSourceCap timer check - TEST.PD.PROT.SRC.3#1:
PASS

start time: 1.36551776 VBusUp time: 1.21303301s Obt time:0.1525s

[PASS] Max = 250ms. Obtained time difference is 152.485ms

Request message response check - TEST.PD.PROT.SRC.3#2:
PASS

UUT respond Accept to Request message

Rev3ChkdSrc:
PASS

tFirstSourceCap timer check - TEST.PD.PROT.SRC.3#1:
PASS

start time: 4.37356695 VBusUp time: 4.2177492s Obt time:0.1558s

[PASS] Max = 250ms. Obtained time difference is 155.818ms

Request message response check - TEST.PD.PROT.SRC.3#2:

PASS

UUT respond Accept to Request message

34. TEST.PD.PROT.SRC.4 Reject Request (Click to View Protocol Trace)

PASS

Rev2Src:

PASS

PDO#1:

PASS

tFirstSourceCap timer check - TEST.PD.PROT.SRC.4#1:

PASS

start time: 1.31780471 VBusUp time: 1.15615421s Obt time:0.1617s

[PASS] Max = 250ms. Obtained time difference is 161.651ms

Reject check - TEST.PD.PROT.SRC.4#2:

PASS

UUT sent Reject message at Protocol index 23

Rev3ChkdSrc:

PASS

PDO#1:

PASS

tFirstSourceCap timer check - TEST.PD.PROT.SRC.4#1:

PASS

start time: 6.35763511 VBusUp time: 6.19431811s Obt time:0.1633s

[PASS] Max = 250ms. Obtained time difference is 163.317ms

Reject check - TEST.PD.PROT.SRC.4#2:

PASS

UUT sent Reject message at Protocol index 47

35. TEST.PD.PROT.SRC.5 Reject Request Invalid Object Position (Click to View Protocol Trace)

PASS

Rev2Src:

PASS

Source_Cap check - TEST.PD.PROT.SRC.5#1:

PASS

start time: 1.3126143 VBusUp time: 1.15346355s Obt time:0.1592s

[PASS] Max = 250ms. Obtained time difference is 159.151ms

Reject check - TEST.PD.PROT.SRC.5#2:

PASS

UUT sent Reject message at protocol index 23

Rev3ChkdSrc:

PASS

Source_Cap check - TEST.PD.PROT.SRC.5#1:

PASS

start time: 6.32352373 VBusUp time: 6.16103998s Obt time:0.1625s

[PASS] Max = 250ms. Obtained time difference is 162.484ms

Reject check - TEST.PD.PROT.SRC.5#2:

PASS

UUT sent Reject message at protocol index 47

36. TEST.PD.PROT.SRC.6 Atomic Message Sequence – Request (Click to View Protocol Trace)

PASS

Rev2Src:
PASS
tFirstSourceCap timer check - TEST.PD.PROT.SRC.6#1:
PASS
start time: 1.31832525 VBusUp time: 1.157508s Obt time:0.1608s
[PASS] Max = 250ms. Obtained time difference is 160.817ms
tProtErrSoftReset timer check - TEST.PD.PROT.SRC.6#2:
PASS
UUT sent SoftReset message received within tSoftReset_Max 0.015s.Protocol index #23
tTypeCSinkWaitCap_Max check - TEST.PD.PROT.SRC.6#3:
PASS
UUT sent Source_Cap message after Soft_Reset within tTypeCSinkWaitCap_Max 0.62s.Protocol index #27
Tester sent Accept message
Rev3ChkdSrc:
PASS
tFirstSourceCap timer check - TEST.PD.PROT.SRC.6#1:
PASS
start time: 4.32256497 VBusUp time: 4.16341422s Obt time:0.1592s
[PASS] Max = 250ms. Obtained time difference is 159.151ms
tProtErrSoftReset timer check - TEST.PD.PROT.SRC.6#2:
PASS
UUT sent SoftReset message received within tSoftReset_Max 0.015s.Protocol index #58
tTypeCSinkWaitCap_Max check - TEST.PD.PROT.SRC.6#3:
PASS
UUT sent Source_Cap message after Soft_Reset within tTypeCSinkWaitCap_Max 0.62s.Protocol index #62
Tester sent Accept message

37. TEST.PD.PROT.SRC.7 DR_Swap (Click to View Protocol Trace)

PASS
COMMON.PROC.BU.1:
PASS
COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src:
PASS
First source capability timer - COMMON.PROC.BU.1#1:
PASS
Vbus up time: 1.142s and SourceCap time: 1.33s at protocol index #16
[PASS] Max = 250ms. Obtained time difference is 187.481ms
DUT responded with accept message - COMMON.PROC.BU.1#2:
PASS
Packet20
tSrcTransReq timer check - COMMON.PROC.BU.1#3:
PASS
[PASS] Max = 325ms. Obtained time difference is 40.431ms
Packet 22
COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:
PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 7.642s and SourceCap time: 7.825s at protocol index #52

[PASS] Max = 250ms. Obtained time difference is 183.315ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet56

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.044ms

Packet 58

Rev2Src:

PASS

DR_Swap Response Check - TEST.PD.PROT.SRC.7#1:

PASS

UUT respond Accept to DR_Swap message and DR_Swap_To_UFP_Supported field is Yes

DR_Swap Response Check - TEST.PD.PROT.SRC.7#2:

PASS

UUT respond Accept to DR_Swap message and DR_Swap_To_DFP_Supported field is Yes

Rev3ChkdSrc:

PASS

DR_Swap Response Check - TEST.PD.PROT.SRC.7#1:

PASS

UUT respond Accept to DR_Swap message and DR_Swap_To_UFP_Supported field is Yes

DR_Swap Response Check - TEST.PD.PROT.SRC.7#2:

PASS

UUT respond Accept to DR_Swap message and DR_Swap_To_DFP_Supported field is Yes

38. TEST.PD.PROT.SRC.8 VCONN_Swap Response (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 1.118s and SourceCap time: 1.303s at protocol index #16

[PASS] Max = 250ms. Obtained time difference is 184.148ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.438ms

Packet 22

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 5.63s and SourceCap time: 5.819s at protocol index #48

[PASS] Max = 250ms. Obtained time difference is 189.148ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet52

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.229ms

Packet 54

Rev2Src:

PASS

VCONN_Swap response check - TEST.PD.PROT.SRC.8#1:

PASS

UUT respond Reject to VCONN_Swap message at protocol index 30 and VCONN_Swap_To_Off_Supported field is NO

NA tVONNSourceOff timer check - TEST.PD.PROT.SRC.8#2:

NA Second VCONN_Swap response check - TEST.PD.PROT.SRC.8#3:

NA PS_RDY check - TEST.PD.PROT.SRC.8#4:

NA VCONN present check - TEST.PD.PROT.SRC.8#5:

NA Third VCONN_Swap response check - TEST.PD.PROT.SRC.8#6:

NA PS_RDY holding check - TEST.PD.PROT.SRC.8#7:

Rev3ChkdSrc:

PASS

VCONN_Swap response check - TEST.PD.PROT.SRC.8#1:

PASS

UUT respond Not_Supported to VCONN_Swap message at protocol index 62 and VCONN_Swap_To_Off_Supported field is NO

NA tVONNSourceOff timer check - TEST.PD.PROT.SRC.8#2:

NA Second VCONN_Swap response check - TEST.PD.PROT.SRC.8#3:

NA PS_RDY check - TEST.PD.PROT.SRC.8#4:

NA VCONN present check - TEST.PD.PROT.SRC.8#5:

NA Third VCONN_Swap response check - TEST.PD.PROT.SRC.8#6:

NA PS_RDY holding check - TEST.PD.PROT.SRC.8#7:

39. TEST.PD.PROT.SRC.9 PR_Swap Response (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 1.172s and SourceCap time: 1.357s at protocol index #16

[PASS] Max = 250ms. Obtained time difference is 184.982ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 39.485ms

Packet 22

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 7.638s and SourceCap time: 7.825s at protocol index #83

[PASS] Max = 250ms. Obtained time difference is 186.648ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet87

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.234ms

Packet 89

Rev2Src:

PASS

PR_Swap response check - TEST.PD.PROT.SRC.9#1:

PASS

UUT respond Accept to PR_Swap message.The VIF field PD_Port_Type is DRP.The VIF field Accepts_PR_Swap_As_Src is YES at protocol index 30.

UUT PS_RDY vSafe0V check - TEST.PD.PROT.SRC.9#2:

PASS

UUT respond PS_RDY message to PR_Swap after VBUS voltage to vSafe0V(0V - 0.8V).The present voltage is 0.0586V at protocol index 33.

tPSSourceOff timer check - TEST.PD.PROT.SRC.9#3:

PASS

UUT respond PS_RDY within tPSSourceOff_Min(750ms) time.The present interval is 0.0727s at protocol index 33.

Tester respond PS_RDY message to UUT message within tNewSrc_Max(275ms).The interval is 0.0415s at protocol index 37.

PD contract check - TEST.PD.PROT.SRC.9#4:

PASS

UUT respond Request to SourceCap message at protocol index 42.

PR_Swap response check - TEST.PD.PROT.SRC.9#5:

PASS

UUT respond Accept to PR_Swap message.The VIF field Accept_PR_Swap_As_Snk is YES.

UUT Rp check - TEST.PD.PROT.SRC.9#6:

PASS

UUT asserts Rp at protocol index 57.

UUT PSRDY vSafe5V check - TEST.PD.PROT.SRC.9#7:

PASS

UUT respond PS_RDY message to Tester message.The present voltage is 5.0563V

tPSSourceOn timer check - TEST.PD.PROT.SRC.9#8:

PASS

UUT respond PS_RDY message to Tester message within

tPSSourceOn_Min(390ms).The interval is 0.095s

tFirstSourceCap timer check - TEST.PD.PROT.SRC.9#9:

PASS

[PASS] Min= 20ms - Max = 250ms. Obtained time difference is 196.114ms

Rev3ChkdSrc:

PASS

PR_Swap response check - TEST.PD.PROT.SRC.9#1:

PASS

UUT respond Accept to PR_Swap message.The VIF field PD_Port_Type is DRP.The VIF field Accepts_PR_Swap_As_Src is YES at protocol index 97.

UUT PS_RDY vSafe0V check - TEST.PD.PROT.SRC.9#2:

PASS

UUT respond PS_RDY message to PR_Swap after VBUS voltage to vSafe0V(0V - 0.8V).The present voltage is 0.0652V at protocol index 99.

tPSSourceOff timer check - TEST.PD.PROT.SRC.9#3:

PASS

UUT respond PS_RDY within tPSSourceOff_Min(750ms) time.The present interval is 0.0737s at protocol index 99.

Tester respond PS_RDY message to UUT message within tNewSrc_Max(275ms).The interval is 0.0426s at protocol index 103.

PD contract check - TEST.PD.PROT.SRC.9#4:

PASS

UUT respond Request to SourceCap message at protocol index 108.

PR_Swap response check - TEST.PD.PROT.SRC.9#5:

PASS

UUT respond Accept to PR_Swap message.The VIF field Accept_PR_Swap_As_Snk is YES.

UUT Rp check - TEST.PD.PROT.SRC.9#6:

PASS

UUT asserts Rp at protocol index 128.

UUT PSRDY vSafe5V check - TEST.PD.PROT.SRC.9#7:

PASS

UUT respond PS_RDY message to Tester message.The present voltage is 5.0638V

tPSSourceOn timer check - TEST.PD.PROT.SRC.9#8:

PASS

UUT respond PS_RDY message to Tester message within tPSSourceOn_Min(390ms).The interval is 0.0864s

tFirstSourceCap timer check - TEST.PD.PROT.SRC.9#9:

PASS

[PASS] Min= 20ms - Max = 250ms. Obtained time difference is 191.837ms

40. TEST.PD.PROT.SRC.10 PR_Swap – PSSourceOnTimer Timeout

PASS (Click to View Protocol Trace)

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 1.175s and SourceCap time: 1.363s at protocol index #16

[PASS] Max = 250ms. Obtained time difference is 187.762ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.112ms

Packet 22

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 5.649s and SourceCap time: 5.834s at protocol index #71

[PASS] Max = 250ms. Obtained time difference is 184.404ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet75

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.418ms

Packet 77

Rev2Src:

PASS

PR_Swap response check - TEST.PD.PROT.SRC.10#1:

PASS

UUT respond Accept to PR_Swap message.The VIF field PD_Port_Type is set to DRP

PS_RDY message check - TEST.PD.PROT.SRC.10#2:

PASS

PS_RDY message recieved at -0.0014 V

UUT sent PS_RDY message to PR_Swap response after VBUS voltage is with in vSafe0V(0V-0.8V)

UUT sent PS_RDY within tSrcTransition_Max(35ms) + tSrcSwapStdby_Max(650ms) time.The time interval is 0.0737s, start time 2.2831s, stop time 2.3568s

Hard_Reset message check - TEST.PD.PROT.SRC.10#3:

PASS

UUT sent Type-C Error Recovery within tPSSourceOn[390ms -480ms].The time interval is 0.4391s

Rev3ChkdSrc:

PASS

PR_Swap response check - TEST.PD.PROT.SRC.10#1:

PASS

UUT respond Accept to PR_Swap message.The VIF field PD_Port_Type is set to DRP

PS_RDY message check - TEST.PD.PROT.SRC.10#2:

PASS

PS_RDY message recieved at -0.0014 V

UUT sent PS_RDY message to PR_Swap response after VBUS voltage is with in vSafe0V(0V-0.8V)

UUT sent PS_RDY within tSrcTransition_Max(35ms) + tSrcSwapStdby_Max(650ms) time.The time interval is 0.0753s, start time 6.7931s, stop time 6.8684s

Hard_Reset message check - TEST.PD.PROT.SRC.10#3:

PASS

UUT sent Type-C Error Recovery within tPSSourceOn[390ms -480ms].The time interval is 0.439s

41. TEST.PD.PROT.SRC.11 Unexpected Message Received in Ready State (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 1.132s and SourceCap time: 1.317s at protocol index #16

[PASS] Max = 250ms. Obtained time difference is 184.982ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.193ms

Packet 22

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 4.641s and SourceCap time: 4.824s at protocol index #57

[PASS] Max = 250ms. Obtained time difference is 183.315ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet61

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 39.521ms

Packet 63

Rev2Src:

PASS

Soft_Reset check - TEST.PD.PROT.SRC.11#1:

PASS

UUT is sent SoftReset message within tProtErrSoftReset_Max(15ms).The obtained interval is 0.0031s.Protocol index #30

Soft_Reset check - TEST.PD.PROT.SRC.11#1:

PASS

UUT is sent SoftReset message within tProtErrSoftReset_Max(15ms).The obtained interval is 0.0031s.Protocol index #30

Rev3ChkdSrc:

PASS

Soft_Reset check - TEST.PD.PROT.SRC.11#1:

PASS

UUT is sent SoftReset message within tProtErrSoftReset_Max(15ms).The obtained interval is 0.0033s.Protocol index #71

Soft_Reset check - TEST.PD.PROT.SRC.11#1:

PASS

UUT is sent SoftReset message within tProtErrSoftReset_Max(15ms).The obtained interval is 0.0033s.Protocol index #71

42. TEST.PD.PROT.SRC.12 Get_Sink_Cap Response (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 1.161s and SourceCap time: 1.349s at protocol index #16

[PASS] Max = 250ms. Obtained time difference is 188.315ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 39.759ms

Packet 22

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 3.679s and SourceCap time: 3.865s at protocol index #47

[PASS] Max = 250ms. Obtained time difference is 185.815ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet51

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 39.911ms

Packet 53

Rev2Src:

PASS

Get_Sink_Cap response check - TEST.PD.PROT.SRC.12#1:

PASS

UUT respond SinkCap to Get_Sink_Cap message.Protocol index #30

Rev3ChkdSrc:

PASS

Get_Sink_Cap response check - TEST.PD.PROT.SRC.12#1:

PASS

UUT respond SinkCap to Get_Sink_Cap message.Protocol index

#61

43. TEST.PD.PROT.SRC.13 PR Swap GoodCRC not sent in Response to PS_RDY (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 1.128s and SourceCap time: 1.314s at protocol index #16

[PASS] Max = 250ms. Obtained time difference is 186.648ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.039ms

Packet 22

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 5.642s and SourceCap time: 5.825s at protocol index #76

[PASS] Max = 250ms. Obtained time difference is 183.315ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet80

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.593ms

Packet 82

Rev2Src:

PASS

PR_Swap response check - TEST.PD.PROT.SRC.13#1:

PASS

UUT respond Accept to PR_Swap message.The VIF field PD_Port_Type is set to DRP

PS_RDY message check - TEST.PD.PROT.SRC.13#2:

PASS

UUT sent PS_RDY message to PR_SWap response after VBUS voltage to vSafe0V(0V-0.8V).The present voltage is 0.3453V.Protocol index #35

UUT sent PS_RDY within tSrcTransition_Max(35ms) + tSrcSwapStdby_Max(650ms) time.The time interval is 0.0797s.Protocol index #35

USB Type-C Error_Recovery check - TEST.PD.PROT.SRC.13#3:

PASS

Expected nRetryCount is 3.Obtained retry count is 3

DUT response time:(0.0376 mS),spec limit time interval is:[<= 15.000000 mS]

Rev3ChkdSrc:

PASS

PR_Swap response check - TEST.PD.PROT.SRC.13#1:
PASS

UUT respond Accept to PR_Swap message.The VIF field PD_Port_Type is set to DRP

PS_RDY message check - TEST.PD.PROT.SRC.13#2:
PASS

UUT sent PS_RDY message to PR_SWap response after VBUS voltage to vSafe0V(0V-0.8V).The present voltage is 0.3319V.Protocol index #95

UUT sent PS_RDY within tSrcTransition_Max(35ms) + tSrcSwapStdby_Max(650ms) time.The time interval is 0.0794s.Protocol index #95

USB Type-C Error_Recovery check - TEST.PD.PROT.SRC.13#3:
PASS

Expected nRetryCount is 2.Obtained retry count is 2

DUT response time:(5.84444 mS),spec limit time interval is:[<= 15.000000 mS]

44. TEST.PD.PROT.SRC3.1 SourceCapabilityTimer Timeout (Click to View Protocol Trace)
PASS

Rev3ChkdSrc:
PASS

tFirstSourceCap timer check - TEST.PD.PROT.SRC3.1#1:
PASS

start time: 1.32374023 VBusUp time: 1.16542273s Obt time:0.1583s

[PASS] Max = 250ms. Obtained time difference is 158.318ms

tTypeCSendSourceCap timer check - TEST.PD.PROT.SRC3.1#2:
PASS

SourceCap[1-2]:Min= 0ms - Max= 1.295ms.Obtained value 1.0042ms

SourceCap[2-3]:Min= 0ms - Max= 1.295ms.Obtained value 1.0042ms

SourceCap[3-4]:Min= 100.9ms - Max= 201.1ms.Obtained value 155.73146ms

SourceCap[4-5]:Min= 0ms - Max= 1.295ms.Obtained value 1.0042ms

45. TEST.PD.PROT.SRC3.2 SenderResponseTimer Timeout (Click to View Protocol Trace)
PASS

Rev3ChkdSrc:
PASS

Source_Cap check - TEST.PD.PROT.SRC3.2#1:
PASS

start time: 1.34140959 VBusUp time: 1.18225884s Obt time:0.1592s

[PASS] Max = 250ms. Obtained time difference is 159.151ms

Hard_Reset check - TEST.PD.PROT.SRC3.2#2:
PASS

DUT sent Hard_Reset message within tSenderResponse Min(27ms) and Max(33ms) timer.The obtained time interval is 0.0293s

46. TEST.PD.PROT.SRC3.3 Get_Source_Cap_Extended Response (Click to View Protocol Trace)
PASS

COMMON.PROC.BU.1:
PASS

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:
PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 1.176s and SourceCap time: 1.362s at protocol index #17

[PASS] Max = 250ms. Obtained time difference is 186.648ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet21

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.284ms

Packet 23

COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 5.64s and SourceCap time: 5.827s at protocol index #48

[PASS] Max = 250ms. Obtained time difference is 187.481ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet52

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.073ms

Packet 54

Rev3ChkdSrc:

PASS

Source_Cap check - [TEST.PD.PROT.SRC3.3#1:

PASS

UUT respond Source_Cap_Extended to Get_Source_Cap_Extended message.

Rev3UnchkdSrc:

PASS

Source_Cap check - [TEST.PD.PROT.SRC3.3#1:

PASS

UUT respond Source_Cap_Extended to Get_Source_Cap_Extended message.

47. TEST.PD.PROT.SRC3.4 Alert Response Source Input Change (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 1.131s and SourceCap time: 1.316s at protocol index #16

[PASS] Max = 250ms. Obtained time difference is 184.982ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 39.897ms

Packet 22

COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 4.641s and SourceCap time: 4.827s at protocol index #45

[PASS] Max = 250ms. Obtained time difference is 185.815ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet49

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.078ms

Packet 51

Rev3ChkdSrc:

PASS

UUT is not respond to Alert message.

Rev3UnchkdSrc:

PASS

UUT is not respond to Alert message.

48. TEST.PD.PROT.SRC3.5 Alert Response Battery Status Change (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 1.148s and SourceCap time: 1.334s at protocol index #16

[PASS] Max = 250ms. Obtained time difference is 185.815ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.114ms

Packet 22

COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 4.244s and SourceCap time: 4.425s at protocol index #45

[PASS] Max = 250ms. Obtained time difference is 180.815ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet49

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.045ms
Packet 51

Rev3ChkdSrc:

PASS

Get_Battery_Status check - TEST.PD.PROT.SRC3.5#1:

PASS

UUT is not respond to Alert message

Rev3UnchkdSrc:

PASS

Get_Battery_Status check - TEST.PD.PROT.SRC3.5#1:

PASS

UUT is not respond to Alert message

49. TEST.PD.PROT.SRC3.6 Soft_Reset Sent when SinkTxOK (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 1.138s and SourceCap time: 1.322s at protocol index #16

[PASS] Max = 250ms. Obtained time difference is 183.315ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.894ms
Packet 22

Rev3ChkdSrc:

PASS

Soft_Reset check - TEST.PD.PROT.SRC3.6#1:

PASS

UUT is respond message within tReceiveMax(1.1ms) + tSoftResetMax(15ms).The interval is 0.0026s

NA 50. TEST.PD.PROT.SRC3.7 Get_PPS_Status Response (Click to View Protocol Trace)

UUT does not support PPS APDO in Source Caps

NA 51. TEST.PD.PROT.SRC3.8 SourcePPSCommTimer Deadline (Click to View Protocol Trace)

UUT does not support PPS APDO in Source Caps

NA 52. TEST.PD.PROT.SRC3.9 SourcePPSCommTimer Timeout (Click to View Protocol Trace)

UUT does not support PPS APDO in Source Caps

NA 53. TEST.PD.PROT.SRC3.10 SourcePPSCommTimer Stopped (Click to View Protocol Trace)

UUT does not support PPS APDO in Source Caps

54. TEST.PD.PROT.SRC3.11 GoodCRC Specification Revision

PASS Compatibility (Click to View Protocol Trace)

Rev3ChkdSrc:

PASS

1.SourceCap Check - TEST.PD.PROT.SRC3.11#1:

PASS

1.GoodCRC Specification Revision with 00b -

PASS TEST.PD.PROT.SRC3.11#2:

2.SourceCap Check - TEST.PD.PROT.SRC3.11#1:

PASS

2.GoodCRC Specification Revision with 01b -

PASS TEST.PD.PROT.SRC3.11#2:

3.SourceCap Check - TEST.PD.PROT.SRC3.11#1:

PASS

3.GoodCRC Specification Revision with 10b -

PASS TEST.PD.PROT.SRC3.11#2:

55. TEST.PD.PROT.SRC3.12 FR Swap Without Signaling (Click to View

PASS Protocol Trace)

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 1.145s and SourceCap time: 1.331s at protocol index #16

[PASS] Max = 250ms. Obtained time difference is 186.648ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.402ms

Packet 22

Rev3ChkdSrc:

PASS

FR_Swap response check - TEST.PD.PROT.SRC3.12#1:

PASS

DUT respond Not_Supported to FR_Swap message

56. TEST.PD.PROT.SRC3.13 Cable Type Detection (Click to View

PASS Protocol Trace)

Rev3ChkdSrc:

PASS

Source_Cap PDO check - TEST.PD.PROT.SRC3.13#1:

PASS

UUT sent SourceCap message.Protocol index #19

UUT SourceCap message offering current <=3A or voltage <=20V

Source_Cap PDO check - TEST.PD.PROT.SRC3.13#2:

PASS

UUT sent SourceCap message.Protocol index #39

UUT SourceCap message offering current <=3A or voltage <=20V

Source_Cap PDO check - TEST.PD.PROT.SRC3.13#3:
PASS

UUT sent SourceCap message.Protocol index #59
UUT SourceCap message offering current <=3A or voltage <=20V

57. TEST.PD.PROT.SRC3.14 Source Info (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.1:
PASS

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:
PASS

First source capability timer - COMMON.PROC.BU.1#1:
PASS

Vbus up time: 1.168s and SourceCap time: 1.351s at protocol index #16
[PASS] Max = 250ms. Obtained time difference is 182.482ms

DUT responded with accept message - COMMON.PROC.BU.1#2:
PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:
PASS

[PASS] Max = 325ms. Obtained time difference is 40.123ms
Packet 22

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:
PASS

First source capability timer - COMMON.PROC.BU.1#1:
PASS

Vbus up time: 3.677s and SourceCap time: 3.858s at protocol index #47
[PASS] Max = 250ms. Obtained time difference is 180.815ms

DUT responded with accept message - COMMON.PROC.BU.1#2:
PASS

Packet51

tSrcTransReq timer check - COMMON.PROC.BU.1#3:
PASS

[PASS] Max = 325ms. Obtained time difference is 40.504ms
Packet 53

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:
PASS

First source capability timer - COMMON.PROC.BU.1#1:
PASS

Vbus up time: 6.227s and SourceCap time: 6.415s at protocol index #78
[PASS] Max = 250ms. Obtained time difference is 187.481ms

DUT responded with accept message - COMMON.PROC.BU.1#2:
PASS

Packet82

tSrcTransReq timer check - COMMON.PROC.BU.1#3:
PASS

[PASS] Max = 325ms. Obtained time difference is 40.741ms
Packet 84

COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 8.777s and SourceCap time: 8.963s at protocol index #109

[PASS] Max = 250ms. Obtained time difference is 185.815ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet113

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.56ms

Packet 115

COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 11.321s and SourceCap time: 11.506s at protocol index #140

[PASS] Max = 250ms. Obtained time difference is 184.981ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet144

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.646ms

Packet 146

COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 13.868s and SourceCap time: 14.05s at protocol index #171

[PASS] Max = 250ms. Obtained time difference is 181.649ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet175

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 39.592ms

Packet 177

Rev3ChkdSrc:

PASS

First Source_Info field check - TEST.PD.PROT.SRC3.14#1:

PASS

First Get_Source_Info response check - TEST.PD.PROT.SRC3.14#2:

PASS

Tester sent Get_Source_Info message

Packet 28

UUT respond Source_Info message for Get_Source_Info message at protocol index #30

Rev3ChkdSrc:

PASS

Second Get_Source_Info response check - TEST.PD.PROT.SRC3.14#3:

PASS

Tester sent Get_Source_Info message
Packet 59
UUT respond Source_Info message for Get_Source_Info message at protocol index #61

Second Source_Info field check - TEST.PD.PROT.SRC3.14#4:

PASS

Rev3ChkdSrc:

PASS

Third Get_Source_Info response check - TEST.PD.PROT.SRC3.14#5:

PASS

Tester sent Get_Source_Info message
Packet 90
UUT respond Source_Info message for Get_Source_Info message at protocol index #92

Third Source_Info field check - TEST.PD.PROT.SRC3.14#6:

PASS

Rev3UnchkdSrc:

PASS

First Source_Info field check - TEST.PD.PROT.SRC3.14#1:

PASS

First Get_Source_Info response check - TEST.PD.PROT.SRC3.14#2:

PASS

Tester sent Get_Source_Info message
Packet 121
UUT respond Source_Info message for Get_Source_Info message at protocol index #123

Rev3UnchkdSrc:

PASS

Second Get_Source_Info response check - TEST.PD.PROT.SRC3.14#3:

PASS

Tester sent Get_Source_Info message
Packet 152
UUT respond Source_Info message for Get_Source_Info message at protocol index #154

Second Source_Info field check - TEST.PD.PROT.SRC3.14#4:

PASS

Rev3UnchkdSrc:

PASS

Third Get_Source_Info response check - TEST.PD.PROT.SRC3.14#5:

PASS

Tester sent Get_Source_Info message
Packet 183
UUT respond Source_Info message for Get_Source_Info message at protocol index #185

Third Source_Info field check - TEST.PD.PROT.SRC3.14#6:

PASS

58. TEST.PD.PROT.SRC3.15 Alert Response Extended Alert (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:
PASS

First source capability timer - COMMON.PROC.BU.1#1:
PASS

Vbus up time: 1.127s and SourceCap time: 1.314s at protocol index #16

[PASS] Max = 250ms. Obtained time difference is 187.481ms

DUT responded with accept message - COMMON.PROC.BU.1#2:
PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:
PASS

[PASS] Max = 325ms. Obtained time difference is 40.133ms

Packet 22

Rev3ChkdSrc:
PASS

Tester sent Alert message

Packet 28

Accept message check - TEST.PD.PROT.SRC3.15#1:
PASS

Tester sent Request message

Packet 31

UUT responded with Accept message at Protocol Index 33

59. TEST.PD.PROT.SNK.1 Get_Sink_Cap Response (Click to View Protocol Trace)
PASS

COMMON.PROC.BU.2:
PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:
PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:
PASS

SourceCap Packet43

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet45

Rev2Snk:
PASS

Get_Sink_Cap Response Check - TEST.PD.PROT.SNK.1#1:
PASS

DUT sent Sink_Cap message at protocol index 27

Rev3ChkdSnk:
PASS

Get_Sink_Cap Response Check - TEST.PD.PROT.SNK.1#1:
PASS

DUT sent Sink_Cap message at protocol index 61

60. TEST.PD.PROT.SNK.2 Get_Source_Cap Response (Click to View Protocol Trace)
PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:

PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet43

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet45

Rev2Snk:

PASS

Get_Source_Cap Response Check - TEST.PD.PROT.SNK.2#1:

PASS

DUT responded with SourceCap message at protocol index27

Rev3ChkdSnk:

PASS

Get_Source_Cap Response Check - TEST.PD.PROT.SNK.2#1:

PASS

DUT responded with SourceCap message at protocol index61

61. TEST.PD.PROT.SNK.3 SinkWaitCapTimer Deadline (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:

PASS

SourceCap Packet15

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet17

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet50

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet52

Rev2Snk:

PASS

Hard_Reset check - TEST.PD.PROT.SNK.3#1:

PASS

Tester sent Hard_Reset message

Packet 26

Tester sent SourceCap message

Packet 28

Tester transmits SourceCap within tTypeCSinkWaitCap min (0.31) S

UUT sent Request message at protocol index 30

NA Request message check - TEST.PD.PROT.SNK.3#2:

Rev3ChkdSnk:

PASS

Hard_Reset check - TEST.PD.PROT.SNK.3#1:

PASS

Tester sent Hard_Reset message

Packet 66

Tester sent SourceCap message

Packet 69

Tester transmits SourceCap within tTypeCSinkWaitCap min (0.31) S

Tester Rp set to SinkTxNG(1.5A)

UUT sent Request message at protocol index 71

NA Request message check - TEST.PD.PROT.SNK.3#2:

62. TEST.PD.PROT.SNK.4 SinkWaitCapTimer Timeout (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:

PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet51

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet53

Rev2Snk:

PASS

SinkWaitCapTimer Timeout - TEST.PD.PROT.SNK.4#1:

PASS

UUT sent HardReset within 0.47246983s

Rev3ChkdSnk:

PASS

SinkWaitCapTimer Timeout - TEST.PD.PROT.SNK.4#1:

PASS

UUT sent HardReset within 0.4729071s

63. TEST.PD.PROT.SNK.5 SenderResponseTimer Deadline (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:

PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet47

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet49

Rev2Snk:

PASS

SenderResponseTimer Deadline - TEST.PD.PROT.SNK.5#1:

PASS

Tester sent SourceCap message
Packet 25
UUT sent Request message
Packet 27
Tester send an Accept message at tCtsSrcAccept 22.531 ms and Max time 22.76 ms at protocol index #29

Rev3ChkdSnk:

PASS

SenderResponseTimer Deadline - TEST.PD.PROT.SNK.5#1:

PASS

Tester sent SourceCap message
Packet 63
UUT sent Request message
Packet 65
Tester send an Accept message at tCtsSrcAccept 25.53 ms and Max time 25.76 ms at protocol index #67

64. TEST.PD.PROT.SNK.6 SenderResponseTimer Timeout (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:

PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet53

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet55

Rev2Snk:

PASS

SenderResponseTimer Timeout - TEST.PD.PROT.SNK.6#1:

PASS

UUT sent Request message
Packet 27
UUT sent Hard_Reset message
Packet 29
[PASS] Min= 24ms - Max = 30ms. Obtained time difference is 26.869ms

Rev3ChkdSnk:

PASS

SenderResponseTimer Timeout - TEST.PD.PROT.SNK.6#1:

PASS

UUT sent Request message
Packet 71
UUT sent Hard_Reset message
Packet 73
[PASS] Min= 27ms - Max = 33ms. Obtained time difference is 30.28ms

65. TEST.PD.PROT.SNK.7 PSTransitionTimer Timeout (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:

PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet55

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet57

Rev2Snk:

PASS

Request message check - TEST.PD.PROT.SNK.7#1:

PASS

UUT sent Request at protocol index 27

PSTransitionTimer timeout delay check - TEST.PD.PROT.SNK.7#2:

PASS

Hard_Reset is detected within 0.5173s at protocol index 31

Rev3ChkdSnk:

PASS

Request message check - TEST.PD.PROT.SNK.7#1:

PASS

UUT sent Request at protocol index 73

PSTransitionTimer timeout delay check - TEST.PD.PROT.SNK.7#2:

PASS

Hard_Reset is detected within 0.5179s at protocol index 77

66. TEST.PD.PROT.SNK.8 Atomic Message Sequence – Accept (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:

PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:
PASS

SourceCap Packet60

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet62

Rev2Snk:
PASS

UUT Request message check - TEST.PD.PROT.SNK.8#1:
PASS

UUT respond Request to SourceCap message

SoftReset response check - TEST.PD.PROT.SNK.8#2:
PASS

UUT respond SoftReset message within 0.0035 S

UUT Request message check - TEST.PD.PROT.SNK.8#3:
PASS

UUT respond Request to SourceCap message

Rev3ChkdSnk:
PASS

UUT Request message check - TEST.PD.PROT.SNK.8#1:
PASS

UUT respond Request to SourceCap message

SoftReset response check - TEST.PD.PROT.SNK.8#2:
PASS

UUT respond SoftReset message within 0.0026 S

UUT Request message check - TEST.PD.PROT.SNK.8#3:
PASS

UUT respond Request to SourceCap message

67. TEST.PD.PROT.SNK.9 Atomic Message Sequence – PS_RDY (Click to View Protocol Trace)
PASS

COMMON.PROC.BU.2:
PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:
PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:
PASS

SourceCap Packet59

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet61

Rev2Snk:
PASS

UUT Request message check - TEST.PD.PROT.SNK.9#1:
PASS

UUT respond Request to SourceCap message

HardReset check - TEST.PD.PROT.SNK.9#2:
PASS

[PASS] Max = 325ms. Obtained time difference is 320.304ms
Packet 33
UUT respond Hard_Reset message.The obtained interval 0.002572s

Rev3ChkdSnk:

PASS

UUT Request message check - TEST.PD.PROT.SNK.9#1:

PASS

UUT respond Request to SourceCap message

HardReset check - TEST.PD.PROT.SNK.9#2:

PASS

[PASS] Max = 325ms. Obtained time difference is 320.929ms
Packet 84
UUT respond Hard_Reset message.The obtained interval 0.003119s

68. TEST.PD.PROT.SNK.10 DR_Swap Request (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:

PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet48

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet50

Rev2Snk:

PASS

First DR_Swap response check - TEST.PD.PROT.SNK.10#1:

PASS

Tester sent DR_Swap message
Packet 25
UUT sent Accept for DR_Swap message at protocol index 27,In VIF DR_Swap_To_DFP_Supported field updated as YES

Second DR_Swap response check - TEST.PD.PROT.SNK.10#2:

PASS

Tester sent DR_Swap message
Packet 30
UUT sent Accept for DR_Swap message at protocol index 32,In VIF DR_Swap_To_UFP_Supported field updated as YES

Rev3ChkdSnk:

PASS

First DR_Swap response check - TEST.PD.PROT.SNK.10#1:

PASS

Tester sent DR_Swap message
Packet 64
UUT sent Accept for DR_Swap message at protocol index 66,In

VIF DR_Swap_To_DFP_Supported field updated as YES

Second DR_Swap response check - TEST.PD.PROT.SNK.10#2:

PASS

Tester sent DR_Swap message

Packet 74

UUT sent Accept for DR_Swap message at protocol index 76,In VIF DR_Swap_To_UFP_Supported field updated as YES

69. TEST.PD.PROT.SNK.11 VCONN_Swap Request (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:

PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet44

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet46

Rev2Snk:

PASS

VCONN present check - TEST.PD.PROT.SNK.11#1:

PASS

Tester VCONN not present at non CC line.The measured VBUS voltage is 0.00688V.

VCONN_Swap response check - TEST.PD.PROT.SNK.11#2:

PASS

UUT respond Reject to VCONN_Swap message and VCONN_Swap_To_On_Supported field is NO at protocol index 27

UUT PS_RDY message check - TEST.PD.PROT.SNK.11#3:

PASS

UUT respond Reject to VCONN_Swap message and VCONN_Swap_To_On_Supported field is NO at protocol index 27

VCONN present check - TEST.PD.PROT.SNK.11#4:

PASS

UUT respond Reject to VCONN_Swap message and VCONN_Swap_To_On_Supported field is NO at protocol index 27

Second VCONN_Swap response check - TEST.PD.PROT.SNK.11#5:

PASS

UUT respond Reject to VCONN_Swap message and VCONN_Swap_To_On_Supported field is NO at protocol index 27

tVCONNSourceOff timer check - TEST.PD.PROT.SNK.11#6:

PASS

UUT respond Reject to VCONN_Swap message and VCONN_Swap_To_On_Supported field is NO at protocol index 27

Rev3ChkdSnk:

PASS

VCONN present check - TEST.PD.PROT.SNK.11#1:

PASS

Tester VCONN not present at non CC line.The measured VBUS voltage is 0.006567V.

VCONN_Swap response check - TEST.PD.PROT.SNK.11#2:

PASS

UUT respond Not_Supported to VCONN_Swap message and VCONN_Swap_To_On_Supported field is NO at protocol index 62

UUT PS_RDY message check - TEST.PD.PROT.SNK.11#3:

PASS

UUT respond Not_Supported to VCONN_Swap message and VCONN_Swap_To_On_Supported field is NO at protocol index 62

VCONN present check - TEST.PD.PROT.SNK.11#4:

PASS

UUT respond Not_Supported to VCONN_Swap message and VCONN_Swap_To_On_Supported field is NO at protocol index 62

Second VCONN_Swap response check - TEST.PD.PROT.SNK.11#5:

PASS

UUT respond Not_Supported to VCONN_Swap message and VCONN_Swap_To_On_Supported field is NO at protocol index 62

tVCONNSourceOff timer check - TEST.PD.PROT.SNK.11#6:

PASS

UUT respond Not_Supported to VCONN_Swap message and VCONN_Swap_To_On_Supported field is NO at protocol index 62

70. TEST.PD.PROT.SNK.12 PR_Swap – PSSourceOffTimer Timeout

PASS (Click to View Protocol Trace)

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:

PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet62

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet64

Rev2Snk:

PASS

PR_Swap response check - TEST.PD.PROT.SNK.12#1:

PASS

UUT respond Accept to PR_Swap message.The VIF field Accept_PR_Swap_As_Snk is set to YES

USB Type-C Error Recovery check - TEST.PD.PROT.SNK.12#2:

PASS

UUT sent Type-C Error Recovery within tPSSourceOff[750ms -920ms].The time interval is 0.8399s

Rev3ChkdSnk:

PASS

PR_Swap response check - TEST.PD.PROT.SNK.12#1:

PASS

UUT respond Accept to PR_Swap message.The VIF field Accept_PR_Swap_As_Snk is set to YES

USB Type-C Error Recovery check - TEST.PD.PROT.SNK.12#2:

PASS

UUT sent Type-C Error Recovery within tPSSourceOff[750ms -920ms].The time interval is 0.8399s

71. TEST.PD.PROT.SNK.13 PR_Swap – Request SenderResponseTimer Timeout (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:

PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet79

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet81

Rev2Snk:

PASS

PR_Swap response check - TEST.PD.PROT.SNK.13#1:

PASS

UUT respond Accept to PR_Swap message.The VIF field PD_Port_Type is DRP

The VIF field Accepts_PR_Swap_As_Snk is YES

UUT PS_RDY check - TEST.PD.PROT.SNK.13#2:

PASS

UUT sent PS_RDY message after VBUS voltage to vSafe5V(4.75V - 5.5V).The present voltage is 5.085636V

tPSSourceOn timer check - TEST.PD.PROT.SNK.13#3:

PASS

UUT respond PS_RDY within tPSSourceOn_Min(390ms) time.The present interval is 0.39s

tSwapSourceStart timer check - TEST.PD.PROT.SNK.13#4:

PASS

UUT sent SourceCap message after tSwapSourceStart(20ms).Obtained time interval 0.192873s

SourceCap message check - TEST.PD.PROT.SNK.13#5:

PASS

UUT respond SourceCap message to Get_Source_Cap message

HardReset message check - TEST.PD.PROT.SNK.13#6:

PASS

UUT sent Hard_Reset within tSenderResponse(24ms - 30ms).Obtained time interval 0.025532s

Rev3ChkdSnk:

PASS

PR_Swap response check - TEST.PD.PROT.SNK.13#1:
PASS

UUT respond Accept to PR_Swap message.The VIF field PD_Port_Type is DRP

The VIF field Accepts_PR_Swap_As_Snk is YES

UUT PS_RDY check - TEST.PD.PROT.SNK.13#2:
PASS

UUT sent PS_RDY message after VBUS voltage to vSafe5V(4.75V - 5.5V).The present voltage is 5.050806V

tPSSourceOn timer check - TEST.PD.PROT.SNK.13#3:
PASS

UUT respond PS_RDY within tPSSourceOn_Min(390ms) time.The present interval is 0.39s

tSwapSourceStart timer check - TEST.PD.PROT.SNK.13#4:
PASS

UUT sent SourceCap message after tSwapSourceStart(20ms).Obtained time interval 0.192606s

SourceCap message check - TEST.PD.PROT.SNK.13#5:
PASS

UUT respond SourceCap message to Get_Source_Cap message

HardReset message check - TEST.PD.PROT.SNK.13#6:
PASS

UUT sent Hard_Reset within tSenderResponse(27ms - 33ms).Obtained time interval 0.027862s

72. TEST.PD.PROT.SNK.14 Valid Use of GoodCRC on Power up (Click to View Protocol Trace)
PASS

Rev2Snk:
PASS

UUT Response with Request message - TEST.PD.PROT.SNK.14#1:
PASS

UUT respond with a Request message within tReceiverResponse_Max 15ms at protocol index #23

[PASS] Max = 325ms. Obtained time difference is 319.578ms

Packet 27

Rev3ChkdSnk:
PASS

UUT Response with Request message - TEST.PD.PROT.SNK.14#1:
PASS

UUT respond with a Request message within tReceiverResponse_Max 15ms at protocol index #51

[PASS] Max = 325ms. Obtained time difference is 321.93ms

Packet 55

73. TEST.PD.PROT.SNK3.1 Get_Source_Cap_Extended (Click to View Protocol Trace)
PASS

COMMON.PROC.BU.2:
PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:
PASS

SourceCap Packet15

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet17

COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk:
PASS

SourceCap Packet54

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet56

Rev3ChkdSnk:
PASS

Get_Source_Cap_Extended - Unchunked Extended Support 0 -
PASS TEST.PD.PROT.SNK3.1#1:

Source_Cap_Extended Packet33

Rev3UnchkdSnk:
PASS

Get_Source_Cap_Extended - Unchunked Extended Support 1 -
PASS TEST.PD.PROT.SNK3.1#1:

Source_Cap_Extended Packet72

74. TEST.PD.PROT.SNK3.2 Alert Response Source Input Change (Click
PASS to View Protocol Trace)

COMMON.PROC.BU.2:
PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:
PASS

SourceCap Packet15

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet17

Rev3ChkdSnk:
PASS

Alert Response Source Input Change - Unchunked Extended Support
PASS 0 - [TEST.PD.PROT.SNK3.2#1]:

DUT not responded to Alert message

75. TEST.PD.PROT.SNK3.3 Alert Response Battery Status Change
PASS (Click to View Protocol Trace)

COMMON.PROC.BU.2:
PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:
PASS

SourceCap Packet15

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet17

COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk:
PASS

SourceCap Packet52

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet54

Rev3ChkdSnk:
PASS

Alert Response Battery Status Change - Unchunked Extended Support
PASS 0 - [TEST.PD.PROT.SNK3.3#1]:

UUT not responded to Alert message

Rev3UnchkdSnk:

PASS

Alert Response Battery Status Change - Unchunked Extended Support

PASS 1 - [TEST.PD.PROT.SNK3.3#1]:

UUT not responded to Alert message

76. TEST.PD.PROT.SNK3.4 Soft_Reset Sent Regardless of Rp Value

PASS (Click to View Protocol Trace)

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet15

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet17

Rev3ChkdSnk:

PASS

Soft_Reset timing check - [TEST.PD.PROT.SNK3.4#1]:

PASS

77. TEST.PD.PROT.SNK3.5 Sink PPS Normal Operation (Click to View

PASS Protocol Trace)

COMMON.PROC.BU.5:

PASS

COMMON.PROC.BU.5 - REVISION_3_0 Snk:

PASS

[PASS] Max = 250ms. Obtained time difference is 47.495ms

Packet19

[PASS] Max = 325ms. Obtained time difference is 321.927ms

Packet 21

UUT should respond with request - COMMON.PROC.BU.5#1:

PASS

Packet17

Rev3ChkdSnk:

PASS

UUT responded Request for Source_Cap message.

Request message check - [TEST.PD.PROT.SNK3.5#1]:

PASS

PPSRequest message not found after PDC

78. TEST.PD.PROT.SNK3.6 Revision Number Test (Click to View

PASS Protocol Trace)

Rev3ChkdSnk:

PASS

Revision Number Test - [TEST.PD.PROT.SNK3.6#1]:

PASS

79. TEST.PD.PROT.SNK3.7 GoodCRC Specification Revision

PASS Compatibility (Click to View Protocol Trace)

Rev3ChkdSnk:

PASS

GoodCrc revision 1 Response Check - TEST.PD.PROT.SNK3.7#1:

PASS

GoodCrc revision 1 Retransmission check - TEST.PD.PROT.SNK3.7#2:
PASS

GoodCrc revision 2 Response Check - TEST.PD.PROT.SNK3.7#1:
PASS

GoodCrc revision 2 Retransmission check - TEST.PD.PROT.SNK3.7#2:
PASS

GoodCrc revision 3 Response Check - TEST.PD.PROT.SNK3.7#1:
PASS

GoodCrc revision 3 Retransmission check - TEST.PD.PROT.SNK3.7#2:
PASS

80. TEST.PD.PROT.SNK3.9 Alert Response Extended Alert (Click to View Protocol Trace)
PASS

COMMON.PROC.BU.2:
PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:
PASS

SourceCap Packet15

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet17

Rev3ChkdSnk:
PASS

Tester sent Alert message
Packet 31

Request message check - TEST.PD.PROT.SNK3.9#1:
PASS

Tester sent SourceCap message
Packet 39
UUT sent Request message
Packet 41

81. TEST.PD.VDM.SNK.1 Discovery Process and Enter Mode (Click to View Protocol Trace)
PASS

COMMON.PROC.BU.2:
PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:
PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:
PASS

SourceCap Packet47

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet49

Rev2Snk:
PASS

Discover ID request Check - TEST.PD.VDM.SNK.1#1:
PASS

DUT sent Responder_ACK for Discover ID at the protocol index
27

Discover ID response Check - TEST.PD.VDM.SNK.1#2:
PASS
Number of VDOs:
PASS
Product Type is Peripheral and Number of Data Obj is 4
Data_Capable_as_USB_Host_SOP:
PASS
VIF data : YES and DUT data : YES
Data_Capable_as_USB_Device_SOP:
PASS
VIF data : YES and DUT data : YES
Product_Type_UFP_SOP:
PASS
VIF data : Peripheral and DUT data : Peripheral
Modal_Operation_Supported_SOP:
PASS
VIF data : NO and DUT data : NO
Check B25..16 is set to zero:
PASS
B25...16 is set to zero
Cert Sat VDO Check:
PASS
VIF data : 0 and DUT data : 0
Product VDO Check:
PASS
VIF data : 0 and DUT data : 0
VIF data : 0 and DUT data : 0
Discover SVID request Check - TEST.PD.VDM.SNK.1#3:
PASS
DUT sent Responder_NAK for Discover SVID
Discover SVID response Check - TEST.PD.VDM.SNK.1#4:
PASS
Discover Mode for each SVID - TEST.PD.VDM.SNK.1#5:
PASS
Enter and Exit Mode for each Mode - TEST.PD.VDM.SNK.1#6:
PASS
Attention Request - TEST.PD.VDM.SNK.1#7:
PASS
Rev3ChkdSnk:
PASS
Discover ID request Check - TEST.PD.VDM.SNK.1#1:
PASS
DUT sent Responder_ACK for Discover ID at the protocol index
65
Discover ID response Check - TEST.PD.VDM.SNK.1#2:
PASS
Number of VDOs:
PASS
VDM_PRODUCT_Type_UFP Peripheral and VDM_PRODUCT_Type_DFP
Host and the Number of Data Object is 7
Number of Data Object is 7 and the 6th VDO pad is 0's

Data_Capable_as_USB_Host_SOP:
PASS

VIF data : YES and DUT data : YES

Data_Capable_as_USB_Device_SOP:
PASS

VIF data : YES and DUT data : YES

Product_Type_UFP_SOP:
PASS

VIF data : Peripheral and DUT data : Peripheral

Modal_Operation_Supported_SOP:
PASS

VIF data : NO and DUT data : NO

Product_Type_DFP_SOP :
PASS

VIF data : Host and DUT data : Host

ID_Header_Connector_Type:
PASS

VIF data : USB_Type_C_Receptacle and DUT data : USB_Type_C_Receptacle

Check B20..16 is set to zero:
PASS

B20...16 is set to zero

Cert Sat VDO Check:
PASS

VIF data : 0 and DUT data : 0

Product VDO Check:
PASS

VIF data : 0 and DUT data : 0

VIF data : 0 and DUT data : 0

Discover SVID request Check - TEST.PD.VDM.SNK.1#3:
PASS

DUT sent Responder_NAK for Discover SVID

Discover SVID response Check - TEST.PD.VDM.SNK.1#4:
PASS

Discover Mode for each SVID - TEST.PD.VDM.SNK.1#5:
PASS

Enter and Exit Mode for each Mode - TEST.PD.VDM.SNK.1#6:
PASS

Attention Request - TEST.PD.VDM.SNK.1#7:
PASS

82. TEST.PD.VDM.SNK.2 Exit Mode without Entering (Click to View Protocol Trace)
PASS

COMMON.PROC.BU.2:
PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:
PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet43

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet45

Rev2Snk:

PASS

SVID Response Check - TEST.PD.VDM.SNK.2#1:

PASS

[PASS] Min= 0.025ms - Max = 15ms. Obtained time difference is 7.27ms

Modal_Operation_Supported_SOP in VIF : 'NO' and in UUT response : 'Responder_NAK'

Exit Mode Check - TEST.PD.VDM.SNK.2#2:

PASS

Invalid Spec revision

Rev3ChkdSnk:

PASS

SVID Response Check - TEST.PD.VDM.SNK.2#1:

PASS

[PASS] Min= 0.025ms - Max = 15ms. Obtained time difference is 7.327ms

Modal_Operation_Supported_SOP in VIF : 'NO' and in UUT response : 'Responder_NAK'

Exit Mode Check - TEST.PD.VDM.SNK.2#2:

PASS

83. TEST.PD.VDM.SNK.5 DR Swap in Modal Operation (Click to View

PASS Protocol Trace)

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:

PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet43

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet45

Rev2Snk:

PASS

SVID Response Check - TEST.PD.VDM.SNK.5#1:

PASS

Modal_Operation_Supported_SOP in VIF : 'NO' and in UUT response : 'Responder_NAK'

Discover Mode Response Check - TEST.PD.VDM.SNK.5#2:

PASS

Enter Mode Response Check - TEST.PD.VDM.SNK.5#3:

PASS

Enter Mode Ack Check - TEST.PD.VDM.SNK.5#4:

PASS

Rev3ChkdSnk:

PASS

SVID Response Check - TEST.PD.VDM.SNK.5#1:

PASS

Modal_Operation_Supported_SOP in VIF : 'NO' and in UUT response : 'Responder_NAK'

Discover Mode Response Check - TEST.PD.VDM.SNK.5#2:

PASS

Enter Mode Response Check - TEST.PD.VDM.SNK.5#3:

PASS

Enter Mode Ack Check - TEST.PD.VDM.SNK.5#4:

PASS

84. TEST.PD.VDM.SNK.6 Structured VDM Revision Number Test (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:

PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet43

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet45

Rev2Snk:

PASS

PD2 - Discover ID Response Check - TEST.PD.VDM.SNK.6#1:

PASS

Response is sent after tInterFrameGap min but before tVDMReceiverResponse max

DUT responded with Responder_ACK at the protocol index 27

Rev3ChkdSnk:

PASS

PD3 - Discover ID Response Check - TEST.PD.VDM.SNK.6#1:

PASS

Response is sent after tInterFrameGap min but before tVDMReceiverResponse max

DUT responded with Responder_ACK at the protocol index 61

85. TEST.PD.VDM.SNK.7 Unrecognized VID in Unstructured VDM (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:

PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet41

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet43

Rev2Snk:

PASS

PD2 - Unstructured VDM Header Response Check -

PASS TEST.PD.VDM.SNK.7#1:

UUT ignored the Tester initiated Unstructured VDM message at protcol index 25

Rev3ChkdSnk:

PASS

PD3 - Unstructured VDM Header Response Check -

PASS TEST.PD.VDM.SNK.7#1:

UUT respond with Not_Supported for Tester initiated Unstructured VDM message at protcol index 57

NA **86. TEST.PD.VDM.CBL.1 Discovery Process and Enter Mode** (Click to View Protocol Trace)

87. TEST.PD.VDM.SRC.1 Discovery Process and Enter Mode (Click to

PASS View Protocol Trace)

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 1.125s and SourceCap time: 1.307s at protocol index #16

[PASS] Max = 250ms. Obtained time difference is 182.482ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.801ms

Packet 22

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 4.318s and SourceCap time: 4.503s at protocol index #56

[PASS] Max = 250ms. Obtained time difference is 184.982ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet60

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.501ms
Packet 62

Rev2Src:

PASS

Discover ID Response Check - TEST.PD.VDM.SRC.1#1:

PASS

UUT respond to Discover_ID within the min 24ms and max 30ms.Obtained time difference is 4.61663 ms

Discover ID ACK Response Check - TEST.PD.VDM.SRC.1#3:

PASS

Attention Request message - TEST.PD.VDM.SRC.1#4:

PASS

Rev3ChkdSrc:

PASS

Discover ID Response Check - TEST.PD.VDM.SRC.1#2:

PASS

UUT responds with a “Responder_ACK” message at protocol index 76 and VIF field Responds_To_Discov_SOP_DFP = YES, Responds_To_Discov_SOP_UFP = YES and Attempts_Discov_SOP = YES.

Discover ID ACK Check - TEST.PD.VDM.SRC.1#3:

PASS

Data_Capable_as_USB_Host_SOP:

PASS

VIF data : YES and DUT data : YES

Data_Capable_as_USB_Device_SOP:

PASS

VIF data : YES and DUT data : YES

Product_Type_UFP_SOP:

PASS

VIF data : Peripheral and DUT data : Peripheral

Modal_Operation_Supported_SOP:

PASS

VIF data : NO and DUT data : NO

Product_Type_DFP_SOP :

PASS

VIF data : Host and DUT data : Host

ID_Header_Connector_Type:

PASS

VIF data : USB_Type_C_Receptacle and DUT data : USB_Type_C_Receptacle

B20...16 is set to zero:

PASS

USB_VID_SOP:

PASS

VIF data : 344F and DUT data : 344F

Cert Sat VDO Check:

PASS

VIF data : 0 and DUT data : 0

Product VDO Check:

PASS

VIF data : 0 and DUT data : 0

VIF data : 0 and DUT data : 0

Attention Request message - TEST.PD.VDM.SRC.1#4:

PASS

88. TEST.PD.VDM.SRC.2 Invalid Fields – Discover Identity (Click to

PASS View Protocol Trace)

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 1.155s and SourceCap time: 1.338s at protocol index #16

[PASS] Max = 250ms. Obtained time difference is 183.315ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.624ms

Packet 22

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 4.278s and SourceCap time: 4.458s at protocol index #53

[PASS] Max = 250ms. Obtained time difference is 179.982ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet57

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.483ms

Packet 59

Rev2Src:

PASS

Discover_ID Response Check - TEST.PD.VDM.SRC.2#1:

PASS

UUT responded with Responder_NAK at protocol index 36

Rev3ChkdSrc:

PASS

Discover_ID Response Check - TEST.PD.VDM.SRC.2#1:

PASS

UUT responded with Responder_NAK at protocol index 73

NA 89. TEST.PD.VDM.CBL3.1 Revision Number Test (Click to View Protocol Trace)

90. TEST.PD.PS.SRC.1 Multiple Request Messages (Click to View

PASS Protocol Trace)

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 1.149s and SourceCap time: 1.336s at protocol index #16

[PASS] Max = 250ms. Obtained time difference is 187.622ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 39.728ms

Packet 22

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 9.103s and SourceCap time: 9.292s at protocol index #114

[PASS] Max = 250ms. Obtained time difference is 189.536ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet118

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.517ms

Packet 120

Rev2Src:

PASS

Rev2Src sequence starts from protocol index 5

PDO : 1 transition with operating current 0

PDO : 1 transition with operating current 0.25

PDO : 1 transition with operating current 0.5

PDO : 1 transition with operating current 0.75

PDO : 1 transition with operating current 1

PDO : 1 transition with operating current 0.75

PDO : 1 transition with operating current 0.5

PDO : 1 transition with operating current 0.25

PDO : 1 transition with operating current 0

Transition (no PDO change) - Current Decrease -

PASS TEST.PD.PS.SRC.1#1:

Load set to 0.75A: [PASS] Vbus voltage before load decrease: 4.97V , Limit:[4.75V - 5.5V] at Protocol index : 68. Measurement after timestamp : 5.30559520S]

Load set to 0.5A: [PASS] Vbus voltage before load decrease: 5.01V , Limit:[4.75V - 5.5V] at Protocol index : 76. Measurement after timestamp : 5.90959842S]

Load set to 0.25A: [PASS] Vbus voltage before load decrease: 5.05V , Limit:[4.75V - 5.5V] at Protocol index : 84. Measurement after timestamp :

6.51359845S]

Load set to 0A: [PASS] Vbus voltage before load decrease: 5.09V , Limit:[4.75V - 5.5V] at Protocol index : 92. Measurement after timestamp : 7.11759850S]

Transition (no PDO change) - Current Increase - TEST.PD.PS.SRC.1#2:

PASS

Load set to 0.25A: [PASS] Vbus voltage before load increase: 5.05V , Limit:[4.75V - 5.5V] at Protocol index : 36. Measurement after timestamp : 2.88959190S]

Load set to 0.5A: [PASS] Vbus voltage before load increase: 5.01V , Limit:[4.75V - 5.5V] at Protocol index : 44. Measurement after timestamp : 3.49359193S]

Load set to 0.75A: [PASS] Vbus voltage before load increase: 4.97V , Limit:[4.75V - 5.5V] at Protocol index : 52. Measurement after timestamp : 4.09759515S]

Load set to 1A: [PASS] Vbus voltage before load increase: 4.94V , Limit:[4.75V - 5.5V] at Protocol index : 60. Measurement after timestamp : 4.70159198S]

Transition (PDO change) - TEST.PD.PS.SRC.1#3:

PASS

Vbus transition - Slew measurement - TEST.PD.PS.SRC.1#4:

PASS

VSrcValid limit - TEST.PD.PS.SRC.1#5:

PASS

Vbus voltage measurement - TEST.PD.PS.SRC.1#6:

PASS

Validate PS_RDY before Vbus - TEST.PD.PS.SRC.1#7:

PASS

Vbus voltage measurement - TEST.PD.PS.SRC.1#8:

PASS

PPS Transition - Current Decrease - TEST.PD.PS.SRC.1#9:

PASS

Validate Request Sequence - TEST.PD.PS.SRC.1#10:

PASS

DUT responded with Accept at the protocol index 30

Validate PS_RDY message - TEST.PD.PS.SRC.1#11:

PASS

[PASS] Max = 325ms. Obtained time difference is 34.757ms
Packet 32

Validate Source_Capability message - TEST.PD.PS.SRC.1#12:

PASS

Validate PS_RDY message - TEST.PD.PS.SRC.1#13:

PASS

Primary Check:

PASS

Load Check:

PASS

Configured Eload value is 0.25 A at packet index 42 and measured is 0.2677 A at time 2.92936758s

Load Check:

PASS

Configured Eload value is 0.5 A at packet index 50 and measured is 0.5168 A at time 3.53349614s

Load Check:

PASS

Configured Eload value is 0.75 A at packet index 58 and measured is 0.766 A at time 4.1379466s

Load Check:

PASS

Configured Eload value is 1 A at packet index 66 and measured is 1.0153 A at time 4.74117021s

Load Check:

PASS

Configured Eload value is 0.75 A at packet index 72 and measured is 0.7659 A at time 5.31104309s

Load Check:

PASS

Configured Eload value is 0.5 A at packet index 80 and measured is 0.5168 A at time 5.91471665s

Load Check:

PASS

Configured Eload value is 0.25 A at packet index 88 and measured is 0.2677 A at time 6.51876412s

Rev3ChkdSrc:

PASS

Rev3ChkdSrc sequence starts from protocol index 103

PDO : 1 transition with operating current 0

PDO : 1 transition with operating current 0.25

PDO : 1 transition with operating current 0.5

PDO : 1 transition with operating current 0.75

PDO : 1 transition with operating current 1

PDO : 1 transition with operating current 0.75

PDO : 1 transition with operating current 0.5

PDO : 1 transition with operating current 0.25

PDO : 1 transition with operating current 0

Transition (no PDO change) - Current Decrease -

PASS TEST.PD.PS.SRC.1#1:

Load set to 0.75A: [PASS] Vbus voltage before load decrease: 4.97V , Limit:[4.75V - 5.5V] at Protocol index : 166. Measurement after timestamp : 13.2735675S]

Load set to 0.5A: [PASS] Vbus voltage before load decrease: 5.01V , Limit:[4.75V - 5.5V] at Protocol index : 174. Measurement after timestamp : 13.8775676S]

Load set to 0.25A: [PASS] Vbus voltage before load decrease: 5.05V , Limit:[4.75V - 5.5V] at Protocol index : 182. Measurement after timestamp : 14.4815708S]

Load set to 0A: [PASS] Vbus voltage before load decrease: 5.09V , Limit:[4.75V - 5.5V] at Protocol index : 190. Measurement after timestamp : 15.0855709S]

Transition (no PDO change) - Current Increase -

PASS TEST.PD.PS.SRC.1#2:

Load set to 0.25A: [PASS] Vbus voltage before load increase: 5.05V , Limit:[4.75V - 5.5V] at Protocol index : 134. Measurement after timestamp : 10.8575642S]

Load set to 0.5A: [PASS] Vbus voltage before load increase:

5.01V , Limit:[4.75V - 5.5V] at Protocol index : 142. Measurement after timestamp : 11.4615642S]

Load set to 0.75A: [PASS] Vbus voltage before load increase: 4.97V , Limit:[4.75V - 5.5V] at Protocol index : 150. Measurement after timestamp : 12.0655675S]

Load set to 1A: [PASS] Vbus voltage before load increase: 4.94V , Limit:[4.75V - 5.5V] at Protocol index : 158. Measurement after timestamp : 12.6695675S]

Transition (PDO change) - TEST.PD.PS.SRC.1#3:

PASS

Vbus transition - Slew measurement - TEST.PD.PS.SRC.1#4:

PASS

VSrcValid limit - TEST.PD.PS.SRC.1#5:

PASS

Vbus voltage measurement - TEST.PD.PS.SRC.1#6:

PASS

Validate PS_RDY before Vbus - TEST.PD.PS.SRC.1#7:

PASS

Vbus voltage measurement - TEST.PD.PS.SRC.1#8:

PASS

PPS Transition - Current Decrease - TEST.PD.PS.SRC.1#9:

PASS

Validate Request Sequence - TEST.PD.PS.SRC.1#10:

PASS

DUT responded with Accept at the protocol index 128

Validate PS_RDY message - TEST.PD.PS.SRC.1#11:

PASS

[PASS] Max = 325ms. Obtained time difference is 33.645ms
Packet 130

Validate Source_Capability message - TEST.PD.PS.SRC.1#12:

PASS

Validate PS_RDY message - TEST.PD.PS.SRC.1#13:

PASS

Primary Check:

PASS

Load Check:

PASS

Configured Eload value is 0.25 A at packet index 140 and measured is 0.2674 A at time 10.89737256s

Load Check:

PASS

Configured Eload value is 0.5 A at packet index 148 and measured is 0.5166 A at time 11.50124631s

Load Check:

PASS

Configured Eload value is 0.75 A at packet index 156 and measured is 0.7659 A at time 12.10535144s

Load Check:

PASS

Configured Eload value is 1 A at packet index 164 and measured is 1.015 A at time 12.70921753s

Load Check:

PASS

Configured Eload value is 0.75 A at packet index 170 and measured is 0.7661 A at time 13.27845397s

Load Check:

PASS

Configured Eload value is 0.5 A at packet index 178 and measured is 0.5169 A at time 13.88291799s

Load Check:

PASS

Configured Eload value is 0.25 A at packet index 186 and measured is 0.2679 A at time 14.48679706s

91. TEST.PD.PS.SRC.2 PDO Transition (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 1.147s and SourceCap time: 1.33s at protocol index #16

[PASS] Max = 250ms. Obtained time difference is 182.705ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.46ms

Packet 22

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 4.258s and SourceCap time: 4.442s at protocol index #49

[PASS] Max = 250ms. Obtained time difference is 184.107ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet53

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.124ms

Packet 55

Rev2Src:

PASS

PDO Transistion in PD2.0 Mode :

PASS

PDO Transition 1 to 1

Check Accept - TEST.PD.PS.SRC.2#1:

PASS

Check PsRdy - TEST.PD.PS.SRC.2#2:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.46ms
Packet 22

Check Vbus is within the vSrcNew or vPpsNew -
PASS TEST.PD.PS.SRC.2#3:

Vbus transition - TEST.PD.PS.SRC.2#4:
PASS

Vbus transition - TEST.PD.PS.SRC.2#5:
PASS

Vbus transition - TEST.PD.PS.SRC.2#6:
PASS

UUT does not send PS_RDY before the VBUS is within vSrcNew or
PASS vPpsNew - TEST.PD.PS.SRC.2#7:

Check Source Capability matches VIF - TEST.PD.PS.SRC.2#8:
PASS

Check Accept - TEST.PD.PS.SRC.2#9:
PASS

Rev3ChkdSrc:
PASS

PDO Transistion in PD3.0 Mode :
PASS

PDO Transition 1 to 1

Check Accept - TEST.PD.PS.SRC.2#1:
PASS

Check PsRdy - TEST.PD.PS.SRC.2#2:
PASS

[PASS] Max = 325ms. Obtained time difference is 40.124ms
Packet 55

Check Vbus is within the vSrcNew or vPpsNew -
PASS TEST.PD.PS.SRC.2#3:

Vbus transition - TEST.PD.PS.SRC.2#4:
PASS

Vbus transition - TEST.PD.PS.SRC.2#5:
PASS

Vbus transition - TEST.PD.PS.SRC.2#6:
PASS

UUT does not send PS_RDY before the VBUS is within vSrcNew or
PASS vPpsNew - TEST.PD.PS.SRC.2#7:

Check Source Capability matches VIF - TEST.PD.PS.SRC.2#8:
PASS

Check Accept - TEST.PD.PS.SRC.2#9:
PASS

92. TEST.PD.PS.SRC.3 Initial Source PDO Transition Post PR Swap

PASS (Click to View Protocol Trace)

COMMON.PROC.BU.1:
PASS

COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src:
PASS

First source capability timer - COMMON.PROC.BU.1#1:
PASS

Vbus up time: 1.155s and SourceCap time: 1.34s at protocol
index #16

[PASS] Max = 250ms. Obtained time difference is 185.815ms

DUT responded with accept message - COMMON.PROC.BU.1#2:
PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:
PASS

[PASS] Max = 325ms. Obtained time difference is 40.869ms
Packet 22

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:
PASS

First source capability timer - COMMON.PROC.BU.1#1:
PASS

Vbus up time: 20.164s and SourceCap time: 20.349s at protocol index #86

[PASS] Max = 250ms. Obtained time difference is 184.148ms

DUT responded with accept message - COMMON.PROC.BU.1#2:
PASS

Packet90

tSrcTransReq timer check - COMMON.PROC.BU.1#3:
PASS

[PASS] Max = 325ms. Obtained time difference is 39.353ms
Packet 92

Rev2Src:
PASS

PR_Swap Response Check - TEST.PD.PS.SRC.3#1:
PASS

DRP UUT sent Accept for PR_Swap message.

UUT PS_RDY Check - TEST.PD.PS.SRC.3#2:
PASS

UUT respond PS_RDY message to PR_SWap after VBUS voltage to vSafe0V(0V - 0.8V).The present voltage is -0.0014V

Tester PS_RDY Check - TEST.PD.PS.SRC.3#3:
PASS

UUT sent PS_RDY within tSrcTransition_Max(35ms) + tSrcSwapStdby_Max(650ms) time.The time interval is 0.0729s, start time 2.3185s, stop time 2.3914s

Source capability check after PR_SWAP - TEST.PD.PS.SRC.3#4:
PASS

Accept Check for PR_Swap - TEST.PD.PS.SRC.3#5:
PASS

Accept Check for PR_Swap - TEST.PD.PS.SRC.3#6:
PASS

Accept Check for PR_Swap - TEST.PD.PS.SRC.3#7:
PASS

Current drawn by the DUT - TEST.PD.PS.SRC.3#8:
PASS

Supply Type is Fixed

Request Check - TEST.PD.PS.SRC.3#9:
PASS

Accept Check - TEST.PD.PS.SRC.3#10:
PASS

Accept Check - TEST.PD.PS.SRC.3#11:

PASS

Accept Check - TEST.PD.PS.SRC.3#12:

PASS

Current drawn by UUT did not exceed previously contracted current (2.01mA) measured from time 8.11736315s to 8.31736315s

Current drawn by the DUT - TEST.PD.PS.SRC.3#13:

PASS

Supply Type is Fixed

Request Check - TEST.PD.PS.SRC.3#14:

PASS

Tester sent SourceCap message
Packet 63
UUT sent Request message
Packet 65

Accept Check - TEST.PD.PS.SRC.3#17:

PASS

Tester sent Accept message
Packet 67

Current drawn by the DUT - TEST.PD.PS.SRC.3#18:

PASS

Tester sent PS_RDY message
Packet 69
Supply Type is Fixed

Current drawn by the DUT - TEST.PD.PS.SRC.3#19:

PASS

Rev3ChkdSrc:

PASS

PR_Swap Response Check - TEST.PD.PS.SRC.3#1:

PASS

DRP UUT sent Accept for PR_Swap message.

UUT PS_RDY Check - TEST.PD.PS.SRC.3#2:

PASS

UUT respond PS_RDY message to PR_SWap after VBUS voltage to vSafe0V(0V - 0.8V).The present voltage is -0.0014V

Tester PS_RDY Check - TEST.PD.PS.SRC.3#3:

PASS

UUT sent PS_RDY within tSrcTransition_Max(35ms) + tSrcSwapStdby_Max(650ms) time.The time interval is 0.0752s, start time 21.3477s, stop time 21.4229s

Source capability check after PR_SWAP - TEST.PD.PS.SRC.3#4:

PASS

Accept Check for PR_Swap - TEST.PD.PS.SRC.3#5:

PASS

Accept Check for PR_Swap - TEST.PD.PS.SRC.3#6:

PASS

Accept Check for PR_Swap - TEST.PD.PS.SRC.3#7:

PASS

Current drawn by the DUT - TEST.PD.PS.SRC.3#8:

PASS

Supply Type is Fixed

Request Check - TEST.PD.PS.SRC.3#9:

PASS

Accept Check - TEST.PD.PS.SRC.3#10:
PASS

Accept Check - TEST.PD.PS.SRC.3#11:
PASS

Accept Check - TEST.PD.PS.SRC.3#12:
PASS

Current drawn by UUT did not exceed previously contracted current (2.01mA) measured from time 27.17507167s to 27.37507167s

Current drawn by the DUT - TEST.PD.PS.SRC.3#13:
PASS

Supply Type is Fixed

Request Check - TEST.PD.PS.SRC.3#14:
PASS

Tester sent SourceCap message
Packet 143
UUT sent Request message
Packet 145

Accept Check - TEST.PD.PS.SRC.3#17:
PASS

Tester sent Accept message
Packet 147

Current drawn by the DUT - TEST.PD.PS.SRC.3#18:
PASS

Tester sent PS_RDY message
Packet 149
Supply Type is Fixed

Current drawn by the DUT - TEST.PD.PS.SRC.3#19:
PASS

93. TEST.PD.PS.SRC.4 Source Behavior with Capability Mismatch Bit

PASS (Click to View Protocol Trace)

COMMON.PROC.BU.1:
PASS

COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src:
PASS

First source capability timer - COMMON.PROC.BU.1#1:
PASS

Vbus up time: 1.132s and SourceCap time: 1.314s at protocol index #16

[PASS] Max = 250ms. Obtained time difference is 181.649ms

DUT responded with accept message - COMMON.PROC.BU.1#2:
PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:
PASS

[PASS] Max = 325ms. Obtained time difference is 40.705ms
Packet 22

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:
PASS

First source capability timer - COMMON.PROC.BU.1#1:
PASS

Vbus up time: 4.249s and SourceCap time: 4.435s at protocol index #49

[PASS] Max = 250ms. Obtained time difference is 186.648ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet53

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 39.935ms

Packet 55

Rev2Src:

PASS

PDO Transition in REVISION_2_0 Mode :

PASS

PDO Transition 1 to 1

Check Accept - TEST.PD.PS.SRC.4#1:

PASS

Accept received at protocol index 20

Check PS_RDY - TEST.PD.PS.SRC.4#2:

PASS

PS_RDY received at protocol index 22

Check PS_RDY receive time - TEST.PD.PS.SRC.4#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.705ms

Packet 22

Check Accept - TEST.PD.PS.SRC.4#4:

PASS

Check PS_RDY - TEST.PD.PS.SRC.4#5:

PASS

Check PS_RDY receive time - TEST.PD.PS.SRC.4#6:

PASS

Check SourceCap matches VIF - TEST.PD.PS.SRC.4#7:

PASS

Rev3ChkdSrc:

PASS

PDO Transition in REVISION_3_0 Mode :

PASS

PDO Transition 1 to 1

Check Accept - TEST.PD.PS.SRC.4#1:

PASS

Accept received at protocol index 53

Check PS_RDY - TEST.PD.PS.SRC.4#2:

PASS

PS_RDY received at protocol index 55

Check PS_RDY receive time - TEST.PD.PS.SRC.4#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 39.935ms

Packet 55

Check Accept - TEST.PD.PS.SRC.4#4:

PASS

Check PS_RDY - TEST.PD.PS.SRC.4#5:

PASS

Check PS_RDY receive time - TEST.PD.PS.SRC.4#6:

PASS

Check SourceCap matches VIF - TEST.PD.PS.SRC.4#7:

PASS

94. TEST.PD.PS.SRC.5 Source Hard Reset Test (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 1.115s and SourceCap time: 1.299s at protocol index #16

[PASS] Max = 250ms. Obtained time difference is 184.148ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.678ms

Packet 22

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 5.625s and SourceCap time: 5.808s at protocol index #58

[PASS] Max = 250ms. Obtained time difference is 182.482ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet62

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.013ms

Packet 64

Rev2Src:

PASS

Check VBUS stays within present valid voltage range - TEST.PD.PS.SRC.5#1:

PASS

Vbus stay within present valid voltage range for tPSHardReset min. Measured volt at 2.27724585s

Check VBUS reaches vSafe0V max - TEST.PD.PS.SRC.5#2:

PASS

VBUS reaches vSafe0V max at 2.2980781 S

Check VBUS rises above vSafe0V max - TEST.PD.PS.SRC.5#3:

PASS

VBUS staying below 0.8 V for duration tSrcRecover min

VBUS rise above vSafe0V max after 0.7249935 S. Measured at 3.0230716 S

Check VBUS reaches vSafe5V - TEST.PD.PS.SRC.5#4:

PASS

VBUS reaches vSafe5V within 3.0480691 S

Source Capabilities message - TEST.PD.PS.SRC.5#5:
PASS

DUT sent Src Cap at 3.20553s.Vbus reached vsafe5v 3.02055s.
Tester transmits Source Cap within tFirstSourceCap max
0.18498s

Highest Fixed PDO Contract check - TEST.PD.PS.SRC.5#6:
PASS

DUT has no highest fixed PDO availablity

Check VBUS stays within present valid voltage range -
PASS TEST.PD.PS.SRC.5#7:

Check VBUS reaches vSafe5V max - TEST.PD.PS.SRC.5#8:
PASS

Check VBUS reaches vSafe0V max - TEST.PD.PS.SRC.5#9:
PASS

Check VBUS rises above vSafe0V max - TEST.PD.PS.SRC.5#10:
PASS

Check VBUS reaches vSafe5V - TEST.PD.PS.SRC.5#11:
PASS

Source Capabilities message - TEST.PD.PS.SRC.5#12:
PASS

Rev3ChkdSrc:
PASS

Check VBUS stays within present valid voltage range -
PASS TEST.PD.PS.SRC.5#1:

Vbus stay within present valid voltage range for tPSHardReset
min. Measured volt at 6.79125404s

Check VBUS reaches vSafe0V max - TEST.PD.PS.SRC.5#2:
PASS

VBUS reaches vSafe0V max at 6.81125304 S

Check VBUS rises above vSafe0V max - TEST.PD.PS.SRC.5#3:
PASS

VBUS staying below 0.8 V for duration tSrcRecover min
VBUS rise above vSafe0V max after 0.7249935 S. Measured at
7.53624654 S

Check VBUS reaches vSafe5V - TEST.PD.PS.SRC.5#4:
PASS

VBUS reaches vSafe5V within 7.56124404 S

Source Capabilities message - TEST.PD.PS.SRC.5#5:
PASS

DUT sent Src Cap at 7.71732s.Vbus reached vsafe5v 7.53317s.
Tester transmits Source Cap within tFirstSourceCap max
0.18415s

Highest Fixed PDO Contract check - TEST.PD.PS.SRC.5#6:
PASS

DUT has no highest fixed PDO availablity

Check VBUS stays within present valid voltage range -
PASS TEST.PD.PS.SRC.5#7:

Check VBUS reaches vSafe5V max - TEST.PD.PS.SRC.5#8:
PASS

Check VBUS reaches vSafe0V max - TEST.PD.PS.SRC.5#9:
PASS

Check VBUS rises above vSafe0V max - TEST.PD.PS.SRC.5#10:
PASS

Check VBUS reaches vSafe5V - TEST.PD.PS.SRC.5#11:
PASS

Source Capabilities message - TEST.PD.PS.SRC.5#12:
PASS

95. TEST.PD.PS.SNK.1 PDO Transition (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:
PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:
PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:
PASS

SourceCap Packet61

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet63

Rev2Snk:
PASS

Get_Sink_Cap response check - TEST.PD.PS.SNK.1#1:
PASS

UUT successfully respond to Get_Sink_Cap message

UUT Request message check - TEST.PD.PS.SNK.1#2:
PASS

Contracted current level check - TEST.PD.PS.SNK.1#5:
PASS

Tester sent PS_RDY message
Packet 36
UUT is drawing current 0.448299A.

Current level check(5Sec) - TEST.PD.PS.SNK.1#6:
PASS

UUT Request message check - TEST.PD.PS.SNK.1#7:
PASS

After tSrcTransition_Min iSnkSusp_Max check -
PASS TEST.PD.PS.SNK.1#10:

Current level check(5Sec) - TEST.PD.PS.SNK.1#11:
PASS

UUT Request position check - TEST.PD.PS.SNK.1#12:
PASS

UUT Request PDP check - TEST.PD.PS.SNK.1#13:
PASS

NA EPR Mode Capable bit check - TEST.PD.PS.SNK.1#14:

UUT EPR Mode check - TEST.PD.PS.SNK.1#15:
PASS

SoftReset check - TEST.PD.PS.SNK.1#16:
PASS

Rev3ChkdSnk:
PASS

Get_Sink_Cap response check - TEST.PD.PS.SNK.1#1:
PASS

UUT successfully respond to Get_Sink_Cap message

UUT Request message check - TEST.PD.PS.SNK.1#2:
PASS

Contracted current level check - TEST.PD.PS.SNK.1#5:
PASS

Tester sent PS_RDY message
Packet 93
UUT is drawing current 0.447562A.

Current level check(5Sec) - TEST.PD.PS.SNK.1#6:
PASS

UUT Request message check - TEST.PD.PS.SNK.1#7:
PASS

After tSrcTransition_Min iSnkSusp_Max check -
PASS TEST.PD.PS.SNK.1#10:

Current level check(5Sec) - TEST.PD.PS.SNK.1#11:
PASS

UUT Request position check - TEST.PD.PS.SNK.1#12:
PASS

UUT Request PDP check - TEST.PD.PS.SNK.1#13:
PASS

EPR Mode Capable bit check - TEST.PD.PS.SNK.1#14:
PASS

UUT EPR Mode check - TEST.PD.PS.SNK.1#15:
PASS

SoftReset check - TEST.PD.PS.SNK.1#16:
PASS

UUT didn't initiated the EPR_Mode_Enter AMS and VIF field is EPR_Supported_As_Snk set to NO.

96. TEST.PD.PS.SNK.2 Initial Sink PDO Transition (Click to View Protocol Trace)
PASS

COMMON.PROC.BU.2:
PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:
PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:
PASS

SourceCap Packet66

UUT should respond with request - - COMMON.PROC.BU.2#1:
PASS

Request Packet68

Rev2Snk:
PASS

PR_Swap message response check - TEST.PD.PS.SNK.2#1:
PASS

UUT respond Accept to PR_Swap message.Accepts_PR_Swap_As_Snk field value is YES

UUT vSafe5V check - TEST.PD.PS.SNK.2#2:

PASS

UUT applied vSafe5V before sending PS_RDY.The Obtained VBUS 05.078675V at 3.60837469

UUT tNewSrc check - TEST.PD.PS.SNK.2#3:

PASS

UUT sent PS_RDY within tNewSrc [275ms].Obtained interval 0.100279

UUT Accept message check - TEST.PD.PS.SNK.2#4:

PASS

PDO #1: UUT respond Accept to Request message

tPSTransition timer check - TEST.PD.PS.SNK.2#5:

PASS

PDO #1: UUT sent PS_RDY message within 450ms. The obtained interval 34.9627899999998ms

vSrcNew timer check - TEST.PD.PS.SNK.2#6:

PASS

PDO #1: Measured VBUS voltage at Accept message: 5.09V. Expected range[4.75V ~ 5.5V]

vSrcValid check - TEST.PD.PS.SNK.2#8:

PASS

[PASS]:vSrcValid limits until tSrcSettle_Max(275ms): Obtained voltage = 5.0857V, Expected voltage limit[4.75~5.5].vSrcValid Measured until 4.80423536s

vSrcNew limits check - TEST.PD.PS.SNK.2#9:

PASS

[PASS]: vSrcNew or vPpsNew limits between tSrcSettle_Max(275ms) and tSrcSettle_Max+100ms: Obtained voltage = 5.0857V, Expected voltage limit[4.75~5.5].vSrcNew or vPpsNew Measured from 4.80423536s to 5.17923536s

UUT PS_RDY message check - TEST.PD.PS.SNK.2#10:

PASS

PDO #1: Measured VBUS voltage at PS_RDY 5.09. Expected range[4.75V ~ 5.5V]

Accept check - TEST.PD.PS.SNK.2#11:

PASS

PS_RDY check - TEST.PD.PS.SNK.2#12:

PASS

PS_RDY check - TEST.PD.PS.SNK.2#13:

PASS

Rev3ChkdSnk:

PASS

PR_Swap message response check - TEST.PD.PS.SNK.2#1:

PASS

UUT respond Accept to PR_Swap message.Accepts_PR_Swap_As_Snk field value is YES

UUT vSafe5V check - TEST.PD.PS.SNK.2#2:

PASS

UUT applied vSafe5V before sending PS_RDY.The Obtained VBUS 05.07821V at 9.27204904

UUT tNewSrc check - TEST.PD.PS.SNK.2#3:

PASS

UUT sent PS_RDY within tNewSrc [275ms].Obtained interval 0.095637

UUT Accept message check - TEST.PD.PS.SNK.2#4:

PASS

PDO #1: UUT respond Accept to Request message

tPSTransition timer check - TEST.PD.PS.SNK.2#5:

PASS

PDO #1: UUT sent PS_RDY message within 450ms. The obtained interval 34.1445799999995ms

vSrcNew timer check - TEST.PD.PS.SNK.2#6:

PASS

PDO #1: Measured VBUS voltage at Accept message: 5.09V. Expected range[4.75V ~ 5.5V]

vSrcValid check - TEST.PD.PS.SNK.2#8:

PASS

[PASS]:vSrcValid limits until tSrcSettle_Max(275ms): Obtained voltage = 5.0856V, Expected voltage limit[4.75~5.5].vSrcValid Measured until 10.46641929s

vSrcNew limits check - TEST.PD.PS.SNK.2#9:

PASS

[PASS]: vSrcNew or vPpsNew limits between tSrcSettle_Max(275ms) and tSrcSettle_Max+100ms: Obtained voltage = 5.0858V, Expected voltage limit[4.75~5.5].vSrcNew or vPpsNew Measured from 10.46641929s to 10.84141929s

UUT PS_RDY message check - TEST.PD.PS.SNK.2#10:

PASS

PDO #1: Measured VBUS voltage at PS_RDY 5.09. Expected range[4.75V ~ 5.5V]

Accept check - TEST.PD.PS.SNK.2#11:

PASS

PS_RDY check - TEST.PD.PS.SNK.2#12:

PASS

PS_RDY check - TEST.PD.PS.SNK.2#13:

PASS

97. TEST.PD.PS.SNK.3 Multiple Request Load Test Post PR Swap (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk:

PASS

SourceCap Packet14

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet16

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet130

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet132

Rev2Snk:

PASS

PR_Swap message response check - [TEST.PD.PS.SNK.3#1:

PASS

UUT respond Accept to PR_Swap message.Accepts_PR_Swap_As_Snk field value is YES

UUT vSafe5V check - TEST.PD.PS.SNK.3#2:

PASS

UUT applied vSafe5V before sending PS_RDY

tNewSrc timer check - TEST.PD.PS.SNK.3#3:

PASS

UUT sent PS_RDY within tNewSrc [275ms].Obtained interval 0.094155

Current decrease transition check - TEST.PD.PS.SNK.3#4:

PASS

[PASS]PDO #1[0.75A load]: Measured VBUS voltage after decrease current to new value: 4.97V at time 7.92786721s. Expected range[4.75V ~ 5.5V]

[PASS]PDO #1[0.5A load]: Measured VBUS voltage after decrease current to new value: 5.01V at time 8.55089776s. Expected range[4.75V ~ 5.5V]

[PASS]PDO #1[0.25A load]: Measured VBUS voltage after decrease current to new value: 5.05V at time 9.17331709s. Expected range[4.75V ~ 5.5V]

[PASS]PDO #1[0A load]: Measured VBUS voltage after decrease current to new value: 5.08V at time 9.79628042s. Expected range[4.75V ~ 5.5V]

Current increase transition check - TEST.PD.PS.SNK.3#5:

PASS

[PASS]PDO #1[0.25A load]: Measured VBUS voltage after increase current to new value: 5.05V at time 5.47109888s. Expected range[4.75V ~ 5.5V]

[PASS]PDO #1[0.5A load]: Measured VBUS voltage after increase current to new value: 5.01V at time 6.09372301s. Expected range[4.75V ~ 5.5V]

[PASS]PDO #1[0.75A load]: Measured VBUS voltage after increase current to new value: 4.98V at time 6.71685914s. Expected range[4.75V ~ 5.5V]

[PASS]PDO #1[1A load]: Measured VBUS voltage after increase current to new value: 4.94V at time 7.34051683s. Expected range[4.75V ~ 5.5V]

UUT Accept message check - TEST.PD.PS.SNK.3#12:

PASS

PDO #1[0A load]: UUT respond Accept to Request message
PDO #1[0.25A load]: UUT respond Accept to Request message
PDO #1[0.5A load]: UUT respond Accept to Request message
PDO #1[0.75A load]: UUT respond Accept to Request message
PDO #1[1A load]: UUT respond Accept to Request message
PDO #1[0.75A load]: UUT respond Accept to Request message
PDO #1[0.5A load]: UUT respond Accept to Request message
PDO #1[0.25A load]: UUT respond Accept to Request message
PDO #1[0A load]: UUT respond Accept to Request message

tPSTransition timer check - TEST.PD.PS.SNK.3#13:

PASS

PDO #1[0A load]: UUT respond PS_RDY message within 450ms. The obtained interval 34.6416ms

PDO #1[0.25A load]: UUT respond PS_RDY message within 450ms. The obtained interval 34.7816ms

PDO #1[0.5A load]: UUT respond PS_RDY message within 450ms. The obtained interval 34.461ms

PDO #1[0.75A load]: UUT respond PS_RDY message within 450ms. The obtained interval 34.8926ms

PDO #1[1A load]: UUT respond PS_RDY message within 450ms. The obtained interval 35.279ms

PDO #1[0.75A load]: UUT respond PS_RDY message within 450ms. The obtained interval 34.7248ms

PDO #1[0.5A load]: UUT respond PS_RDY message within 450ms. The obtained interval 35.72ms

PDO #1[0.25A load]: UUT respond PS_RDY message within 450ms. The obtained interval 34.7152ms

PDO #1[0A load]: UUT respond PS_RDY message within 450ms. The obtained interval 35.1822ms

tPSTransition timer check - TEST.PD.PS.SNK.3#14:

PASS

Rev3ChkdSnk:

PASS

PR_Swap message response check - [TEST.PD.PS.SNK.3#1:

PASS

UUT respond Accept to PR_Swap message.Accepts_PR_Swap_As_Snk field value is YES

UUT vSafe5V check - TEST.PD.PS.SNK.3#2:

PASS

UUT applied vSafe5V before sending PS_RDY

tNewSrc timer check - TEST.PD.PS.SNK.3#3:

PASS

UUT sent PS_RDY within tNewSrc [275ms].Obtained interval 0.098725

Current decrease transition check - TEST.PD.PS.SNK.3#4:

PASS

[PASS]PDO #1[0.75A load]: Measured VBUS voltage after decrease current to new value: 4.97V at time 18.56833399s. Expected range[4.75V ~ 5.5V]

[PASS]PDO #1[0.5A load]: Measured VBUS voltage after decrease current to new value: 5.01V at time 19.19158534s. Expected range[4.75V ~ 5.5V]

[PASS]PDO #1[0.25A load]: Measured VBUS voltage after decrease current to new value: 5.05V at time 19.81477907s. Expected range[4.75V ~ 5.5V]

[PASS]PDO #1[0A load]: Measured VBUS voltage after decrease current to new value: 5.08V at time 20.43779361s. Expected range[4.75V ~ 5.5V]

Current increase transition check - TEST.PD.PS.SNK.3#5:

PASS

[PASS]PDO #1[0.25A load]: Measured VBUS voltage after increase current to new value: 5.05V at time 16.11242641s. Expected range[4.75V ~ 5.5V]

[PASS]PDO #1[0.5A load]: Measured VBUS voltage after increase current to new value: 5.01V at time 16.73500256s. Expected range[4.75V ~ 5.5V]

[PASS]PDO #1[0.75A load]: Measured VBUS voltage after increase current to new value: 4.98V at time 17.3578859s. Expected range[4.75V ~ 5.5V]

[PASS]PDO #1[1A load]: Measured VBUS voltage after increase current to new value: 4.94V at time 17.98050683s. Expected range[4.75V ~ 5.5V]

UUT Accept message check - TEST.PD.PS.SNK.3#12:

PASS

PDO #1[0A load]: UUT respond Accept to Request message
PDO #1[0.25A load]: UUT respond Accept to Request message
PDO #1[0.5A load]: UUT respond Accept to Request message
PDO #1[0.75A load]: UUT respond Accept to Request message
PDO #1[1A load]: UUT respond Accept to Request message
PDO #1[0.75A load]: UUT respond Accept to Request message
PDO #1[0.5A load]: UUT respond Accept to Request message
PDO #1[0.25A load]: UUT respond Accept to Request message
PDO #1[0A load]: UUT respond Accept to Request message

tPSTransition timer check - TEST.PD.PS.SNK.3#13:

PASS

PDO #1[0A load]: UUT respond PS_RDY message within 450ms. The obtained interval 34.2774ms
PDO #1[0.25A load]: UUT respond PS_RDY message within 450ms. The obtained interval 35.0726ms
PDO #1[0.5A load]: UUT respond PS_RDY message within 450ms. The obtained interval 35.2206ms
PDO #1[0.75A load]: UUT respond PS_RDY message within 450ms. The obtained interval 35.1408ms
PDO #1[1A load]: UUT respond PS_RDY message within 450ms. The obtained interval 34.4406ms
PDO #1[0.75A load]: UUT respond PS_RDY message within 450ms. The obtained interval 34.7882ms
PDO #1[0.5A load]: UUT respond PS_RDY message within 450ms. The obtained interval 34.844ms
PDO #1[0.25A load]: UUT respond PS_RDY message within 450ms. The obtained interval 34.4638ms
PDO #1[0A load]: UUT respond PS_RDY message within 450ms. The obtained interval 34.4166ms

tPSTransition timer check - TEST.PD.PS.SNK.3#14:

PASS

98. TEST.PD.EPR.SRC3.1 EPR Entry Process - UUT as VCONN Source

PASS (Click to View Protocol Trace)

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 1.129s and SourceCap time: 1.311s at protocol index #16
[PASS] Max = 250ms. Obtained time difference is 182.482ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.488ms
Packet 22

COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 9.641s and SourceCap time: 9.829s at protocol index #64

[PASS] Max = 250ms. Obtained time difference is 187.481ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet68

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 39.225ms

Packet 70

Rev3ChkdSrc:

PASS

Rev3ChkdSrc sequence starts from protocol index 5

EPR Mode check - TEST.PD.EPR.SRC3.1#2:

PASS

Tester sent EPR_Mode Enter message

Packet 32

UUT did respond with Not_Supported at the protocol index 34 and VIF field EPR_Supported_As_Src is NO

Packet 34

Vconn_Swap message - TEST.PD.EPR.SRC3.1#3:

PASS

Discover ID SOP1 message check - TEST.PD.EPR.SRC3.1#4:

PASS

EPR Mode Enter Succeeded message check - TEST.PD.EPR.SRC3.1#5:

PASS

EPR_Source_Capability message check - TEST.PD.EPR.SRC3.1#6:

PASS

Accept message check - TEST.PD.EPR.SRC3.1#7:

PASS

PS_Rdy message check - TEST.PD.EPR.SRC3.1#8:

PASS

Source Cap message check - TEST.PD.EPR.SRC3.1#9:

PASS

Source Cap message Detail check - TEST.PD.EPR.SRC3.1#10:

PASS

Source Cap message Detail check - TEST.PD.EPR.SRC3.1#11:

PASS

Wait response check - TEST.PD.EPR.SRC3.1#12:

PASS

EPR Get Sourcecap Check - TEST.PD.EPR.SRC3.1#13:

PASS

Tester sent Extended_Control EPR_Get_Source_Cap message

Packet 27

UUT responded with Not_Supported.UUT is DRP , VIF field EPR_Supported_As_Src is NO and VIF field EPR_Supported_As_Snk is NO

Rev3UnchkdSrc:

PASS

Rev3UnchkdSrc sequence starts from protocol index 53

EPR Mode check - TEST.PD.EPR.SRC3.1#2:

PASS

Tester sent EPR_Mode Enter message
Packet 80
UUT did respond with Not_Supported at the protocol index 82 and VIF field EPR_Supported_As_Src is NO
Packet 82

Vconn_Swap message - TEST.PD.EPR.SRC3.1#3:

PASS

Discover ID SOP1 message check - TEST.PD.EPR.SRC3.1#4:

PASS

EPR Mode Enter Succeeded message check - TEST.PD.EPR.SRC3.1#5:

PASS

EPR_Source_Capability message check - TEST.PD.EPR.SRC3.1#6:

PASS

Accept message check - TEST.PD.EPR.SRC3.1#7:

PASS

PS_Rdy message check - TEST.PD.EPR.SRC3.1#8:

PASS

Source Cap message check - TEST.PD.EPR.SRC3.1#9:

PASS

Source Cap message Detail check - TEST.PD.EPR.SRC3.1#10:

PASS

Source Cap message Detail check - TEST.PD.EPR.SRC3.1#11:

PASS

Wait response check - TEST.PD.EPR.SRC3.1#12:

PASS

EPR Get Sourcecap Check - TEST.PD.EPR.SRC3.1#13:

PASS

Tester sent Extended_Control EPR_Get_Source_Cap message
Packet 75
UUT responded with Not_Supported.UUT is DRP , VIF field EPR_Supported_As_Src is NO and VIF field EPR_Supported_As_Snk is NO

NA 99. TEST.PD.EPR.SRC3.2 EPR Entry Process - Tester as VCONN Source (Click to View Protocol Trace)

EPR_Supported_As_Src is set to NO in VIF

NA 100. TEST.PD.EPR.SRC3.3 EPR Entry failed - EPR Mode Capable bit not set in RDO (Click to View Protocol Trace)

EPR_Supported_As_Src is set to NO in VIF

NA 101. TEST.PD.EPR.SRC3.4 EPR Entry failed – Tester as VCONN source (Click to View Protocol Trace)

EPR_Supported_As_Src is set to NO in VIF

NA 102. TEST.PD.EPR.SRC3.5 EPR Entry Failed - EPR_Mode(Reserved) message (Click to View Protocol Trace)

EPR_Supported_As_Src is set to NO in VIF

NA 103. TEST.PD.EPR.SRC3.6 EPR Entry Failed - Cable not EPR capable (Click to View Protocol Trace)

EPR_Supported_As_Src is set to NO in VIF

NA 104. TEST.PD.EPR.SRC3.7 EPR Entry Failed - Interrupted by EPR_Get_Sink_Cap message (Click to View Protocol Trace)

EPR_Supported_As_Src is set to NO in VIF

NA 105. TEST.PD.EPR.SRC3.8 EPR mode - Request message response

(Click to View Protocol Trace)

EPR_Supported_As_Src is set to NO in VIF

NA 106. TEST.PD.EPR.SRC3.9 EPR mode - EPR_Get_Source_Cap message (Click to View Protocol Trace)

EPR_Supported_As_Src is set to NO in VIF

PASS 107. TEST.PD.EPR.SRC3.10 SPR mode - EPR_Get_Source_Cap message (Click to View Protocol Trace)

COMMON.PROC.BU.1:

PASS

COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc:

PASS

First source capability timer - COMMON.PROC.BU.1#1:

PASS

Vbus up time: 1.21s and SourceCap time: 1.39s at protocol index #16

[PASS] Max = 250ms. Obtained time difference is 179.982ms

DUT responded with accept message - COMMON.PROC.BU.1#2:

PASS

Packet20

tSrcTransReq timer check - COMMON.PROC.BU.1#3:

PASS

[PASS] Max = 325ms. Obtained time difference is 40.343ms

Packet 22

Rev3ChkSrc:

PASS

EPR Mode Message Response - TEST.PD.EPR.SRC3.10#1:

PASS

Tester sent Extended_Control EPR_Get_Source_Cap message

Packet 27

UUT responded with Not_Supported.UUT is DRP , VIF field EPR_Supported_As_Src is NO and VIF field EPR_Supported_As_Snk is NO at protocol index 29

NA DUT initiates Hard reset - TEST.PD.EPR.SRC3.10#2:

NA 108. TEST.PD.EPR.SRC3.11 EPR Mode Exit by EPR_Mode_Exit message (Click to View Protocol Trace)

EPR_Supported_As_Src is set to NO in VIF

NA 109. TEST.PD.EPR.SRC3.12 EPR mode - Get_Source_Cap message and Request message response (Click to View Protocol Trace)

EPR_Supported_As_Src is set to NO in VIF

NA 110. TEST.PD.EPR.SRC3.13 EPR mode - tSourceEPRKeepAlive Timeout (Click to View Protocol Trace)

EPR_Supported_As_Src is set to NO in VIF

NA 111. TEST.PD.EPR.SRC3.14 EPR mode - EPR_Request with Incorrect copy of PDO (Click to View Protocol Trace)

EPR_Supported_As_Src is set to NO in VIF

NA 112. TEST.PD.EPR.SRC3.15 DiscoverIdentityCounter and DiscoverIdentityTimer check for SOP1 (Click to View Protocol Trace)

EPR_Supported_As_Src is set to NO in VIF

Captive_Cable is set to NO in VIF

NA 113. TEST.PD.EPR.SRC3.16 PR_Swap for the UUT as EPR Source (Click to View Protocol Trace)

EPR_Supported_As_Src is set to NO in VIF

114. TEST.PD.EPR.SNK3.1 EPR Entry Process - Success (Click to View Protocol Trace)

PASS

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet15

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet17

COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk:

PASS

SourceCap Packet52

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet54

Rev3ChkdSnk:

PASS

Rev3ChkdSnk sequence starts from protocol index 5

EPR Mode Capable check - TEST.PD.EPR.SNK3.1#1:

PASS

EPR mode capable field is set to 0 in the Request message sent by UUT at the protocol index 17, VIF field EPR_Supported_As_Snk is set to NO

Voltage value during the Accept at the protocol in index 19:

PASS

Measured voltage value is 5.0004V at time 1.00943422s

Voltage value during the PS_RDY at the protocol in index 21:

PASS

Measured voltage value is 5.0021V at time 1.33243756s

[PASS] Measured Vbus voltage is 5.002V and expected is [Min - 4.5 and Max - 5.5]V

EPR Mode Enter check - TEST.PD.EPR.SNK3.1#2:

PASS

Discover ID SOP1 check - TEST.PD.EPR.SNK3.1#3:

PASS

tSinkEPRKeepAlive.max check - TEST.PD.EPR.SNK3.1#4:

PASS

EPR Keep_Alive message check - TEST.PD.EPR.SNK3.1#5:

PASS

EPR_Request message check - TEST.PD.EPR.SNK3.1#6:

PASS

SourceCap message check - TEST.PD.EPR.SNK3.1#7:

PASS

EPR contract negotiation check - TEST.PD.EPR.SNK3.1#8:

PASS

SPR contract negotiation - TEST.PD.EPR.SNK3.1#9:

PASS

EPR_Source_Capabilities Message check - TEST.PD.EPR.SNK3.1#10:

PASS

Get_EPR_SinkCap Message check - TEST.PD.EPR.SNK3.1#11:

PASS

Tester sent Extended_Control EPR_Get_Sink_Cap message
Packet 25
UUT responded with Not_Supported.UUT is DRP , VIF field EPR_Supported_As_Src is NO and VIF field EPR_Supported_As_Snk is NO

Rev3UnchkdSnk:

PASS

Rev3UnchkdSnk sequence starts from protocol index 42

EPR Mode Capable check - TEST.PD.EPR.SNK3.1#1:

PASS

EPR mode capable field is set to 0 in the Request message sent by UUT at the protocol index 54, VIF field EPR_Supported_As_Snk is set to NO

Voltage value during the Accept at the protocol in index 56:

PASS

Measured voltage value is 5.0014V at time 9.60445322s

Voltage value during the PS_RDY at the protocol in index 58:

PASS

Measured voltage value is 5.0013V at time 9.92745333s
[PASS] Measured Vbus voltage is 5.001V and expected is [Min - 4.5 and Max - 5.5]V

EPR Mode Enter check - TEST.PD.EPR.SNK3.1#2:

PASS

Discover ID SOP1 check - TEST.PD.EPR.SNK3.1#3:

PASS

tSinkEPRKeepAlive.max check - TEST.PD.EPR.SNK3.1#4:

PASS

EPR Keep_Alive message check - TEST.PD.EPR.SNK3.1#5:

PASS

EPR_Request message check - TEST.PD.EPR.SNK3.1#6:

PASS

SourceCap message check - TEST.PD.EPR.SNK3.1#7:

PASS

EPR contract negotiation check - TEST.PD.EPR.SNK3.1#8:

PASS

SPR contract negotiation - TEST.PD.EPR.SNK3.1#9:

PASS

EPR_Source_Capabilities Message check - TEST.PD.EPR.SNK3.1#10:

PASS

Get_EPR_SinkCap Message check - TEST.PD.EPR.SNK3.1#11:

PASS

Tester sent Extended_Control EPR_Get_Sink_Cap message
Packet 62
UUT responded with Not_Supported.UUT is DRP , VIF field EPR_Supported_As_Src is NO and VIF field EPR_Supported_As_Snk is NO

NA **115. TEST.PD.EPR.SNK3.2 EPR Entry Fail tEnterEPR Timer Timeout** (Click to View Protocol Trace)

EPR_Supported_As_Snk is set to NO in VIF

NA **116. TEST.PD.EPR.SNK3.3 EPR Fail by EPR Enter Failed Message** (Click to View Protocol Trace)

EPR_Supported_As_Snk is set to NO in VIF

NA **117. TEST.PD.EPR.SNK3.4 EPR Entry Fail tFirstSourceCap Timer Timeout** (Click to View Protocol Trace)

EPR_Supported_As_Snk is set to NO in VIF

NA 118. TEST.PD.EPR.SNK3.5 EPR Exit by Incorrect EPR Source Cap (Click to View Protocol Trace)

EPR_Supported_As_Snk is set to NO in VIF

NA 119. TEST.PD.EPR.SNK3.6 EPR Exit by EPR Exit Message (Click to View Protocol Trace)

EPR_Supported_As_Snk is set to NO in VIF

NA 120. TEST.PD.EPR.SNK3.8 EPR Exit by Source Cap Message (Click to View Protocol Trace)

EPR_Supported_As_Snk is set to NO in VIF

NA 121. TEST.PD.EPR.SNK3.9 EPR Entry failed due to SourceCap (Click to View Protocol Trace)

EPR_Supported_As_Snk is set to NO in VIF

NA 122. TEST.PD.EPR.SNK3.10 EPR Exit fail due to SinkWaitCapTimer timeout (Click to View Protocol Trace)

EPR_Supported_As_Snk is set to NO in VIF

NA 123. TEST.PD.EPR.SNK3.11 PR_Swap for the UUT as the EPR Sink (Click to View Protocol Trace)

EPR_Supported_As_Snk is set to NO in VIF

NA 124. TEST.PD.PS.EPR.SRC3.1 Multiple EPR Request Load Test (Click to View Protocol Trace)

EPR_Supported_As_Src is set to NO in VIF

NA 125. TEST.PD.PS.EPR.SRC3.2 PDO Transitions in EPR Mode (Click to View Protocol Trace)

EPR_Supported_As_Src is set to NO in VIF

NA 126. TEST.PD.FRS.SRC3.1 Normal Conditions (Click to View Protocol Trace)

NA 127. TEST.PD.FRS.SRC3.2 Provider Only Checks (Click to View Protocol Trace)

NA 128. TEST.PD.FRS.SRC3.3 GoodCRC Not Sent In Response To Accept (Click to View Protocol Trace)

NA 129. TEST.PD.FRS.SRC3.4 GoodCRC Not Sent In Response To PS_RDY (Click to View Protocol Trace)

NA 130. TEST.PD.FRS.SRC3.5 PSSourceOnTimer Deadline (Click to View Protocol Trace)

NA 131. TEST.PD.FRS.SRC3.6 PSSourceOnTimer Timeout (Click to View Protocol Trace)

PASS 132. TEST.PD.FRS.SNK3.1 Normal Conditions (Click to View Protocol Trace)

PASS COMMON.PROC.BU.2:

PASS COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk5V:

SourceCap Packet15

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet17

PASS COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnkHiV:

SourceCap Packet63

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet65

Rev3ChkdSnk5V:

PASS

UUT Get_Sink_Cap check - TEST.PD.FRS.SNK3.1#1:

PASS

The VIF parameter FR_Swap_Type_C_Current_Capability_As_Initial_Sink is FR_Swap_Not_Supported

Tester draws no current after dropped VBUS .Measured Voltage: 04.6779 and Current -00.0884 from 2.75449871 to 2.75469871. Limit <2.5W

VBUS Electrical check - TEST.PD.FRS.SNK3.1#2:

PASS

PDMessage check - TEST.PD.FRS.SNK3.1#3:

PASS

UUT not sending FR_Swap message. The VIF parameter FR_Swap_Type_C_Current_Capability_As_Initial_Sink is FR_Swap_Not_Supported

UUT VBus Supply - TEST.PD.FRS.SNK3.1#8:

PASS

The VIF parameter FR_Swap_Type_C_Current_Capability_As_Initial_Sink is FR_Swap_Not_Supported

UUT does not supply VBUS

Rev3ChkdSnkHiV:

PASS

UUT Get_Sink_Cap check - TEST.PD.FRS.SNK3.1#1:

PASS

The VIF parameter FR_Swap_Type_C_Current_Capability_As_Initial_Sink is FR_Swap_Not_Supported

Tester draws no current after dropped VBUS .Measured Voltage: 04.5466 and Current 00.0035 from 7.76500435 to 7.76520435. Limit <2.5W

VBUS Electrical check - TEST.PD.FRS.SNK3.1#2:

PASS

PDMessage check - TEST.PD.FRS.SNK3.1#3:

PASS

UUT not sending FR_Swap message. The VIF parameter FR_Swap_Type_C_Current_Capability_As_Initial_Sink is FR_Swap_Not_Supported

UUT VBus Supply - TEST.PD.FRS.SNK3.1#8:

PASS

The VIF parameter FR_Swap_Type_C_Current_Capability_As_Initial_Sink is FR_Swap_Not_Supported

UUT does not supply VBUS

NA **133. TEST.PD.FRS.SNK3.2 Normal Conditions, Consumer Only** (Click to View Protocol Trace)

PASS **134. TEST.PD.FRS.SNK3.3 FR_Swap Not Sent** (Click to View Protocol Trace)

VIF field FR_Swap_Type_C_Current_Capability_As_Initial_Sink set to 00b

PASS **135. TEST.PD.FRS.SNK3.4 SendResponseTimer Timeout** (Click to View Protocol Trace)

VIF field FR_Swap_Type_C_Current_Capability_As_Initial_Sink set to 00b

PASS **136. TEST.PD.FRS.SNK3.5 PSSourceOffTimer Deadline** (Click to View Protocol Trace)

VIF field FR_Swap_Type_C_Current_Capability_As_Initial_Sink set to 00b

PASS 137. TEST.PD.FRS.SNK3.6 PSSourceOffTimer Timeout (Click to View Protocol Trace)

VIF field FR_Swap_Type_C_Current_Capability_As_Initial_Sink set to 00b

PASS 138. TEST.PD.FRS.SNK3.7 GoodCRC Not Sent in Response to PS_RDY (Click to View Protocol Trace)

VIF field FR_Swap_Type_C_Current_Capability_As_Initial_Sink set to 00b

PASS 139. TEST.PD.USB4.DRST.1 –Data_Reset command response of UFP UUT (Click to View Protocol Trace)

COMMON.PROC.BU.2:

PASS

COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk:

PASS

SourceCap Packet15

UUT should respond with request - - COMMON.PROC.BU.2#1:

PASS

Request Packet17

Rev3ChkdSnk:

PASS

Data_Reset command response check - TEST.PD.USB4.DRST.1#1:

PASS

Tester sent Data_Reset message

Packet 31

UUT sent Not_Supported message

Packet 33

NA Data_Reset_Complete response check - TEST.PD.USB4.DRST.1#4:

NA Data role check - TEST.PD.USB4.DRST.1#5:

NA 140. TEST.PD.USB4.DRST.2 –Data_Reset command response of UFP UUT, Invalid Sequence (Click to View Protocol Trace)

In VIF Data_Reset_Supported field is NO

NA 141. TEST.PD.USB4.DRST.3 –Data_Reset command response of UFP UUT Sourcing Vconn (Click to View Protocol Trace)

In VIF Data_Reset_Supported field is NO and VCONN_Swap_To_On_Supported field is NO

NA 142. TEST.PD.USB4.DRST.4 –DataReset command response of UFP UUT Sourcing Vconn – Invalid Sequence (Click to View Protocol Trace)

In VIF Data_Reset_Supported field is NO and VCONN_Swap_To_On_Supported field is NO

NA 143. TEST.PD.USB4.DRST.5 –Data_Reset command response of DFP UUT Sourcing Vconn (Click to View Protocol Trace)

In VIF Data_Reset_Supported field is NO

NA 144. TEST.PD.USB4.DRST.6 –Data_Reset command response of DFP UUT, UFP Sourcing Vconn (Click to View Protocol Trace)

In VIF VCONN_Swap_To_Off_Supported field is NO

In VIF Data_Reset_Supported field is NO

NA 145. TEST.PD.USB4.DRST.7 –Data_reset command response of DFP UUT, UFP Sourcing Vconn- VCONNDischargeTimer expiry check (Click to View Protocol Trace)

In VIF VCONN_Swap_To_Off_Supported field is NO

In VIF Data_Reset_Supported field is NO

NA 146. TEST.PD.USB4.EUSB.1 – Enter_USB Message response of UFP UUT-Valid Mode (Click to View Protocol Trace)

In VIF USB4_UFP_Supported field is NONE

NA 147. TEST.PD.USB4.EUSB.2 – Enter_USB Message response of UFP UUT-Invalid Mode (Click to View Protocol Trace)

In VIF USB4_UFP_Supported field is NONE

NA 148. TEST.PD.USB4.EUSB.3 – Enter_USB Flow-USB4 DFP Connected to USB4 UFP using an Active Cable (Click to View Protocol Trace)

In VIF USB4_DFP_Supported field is NONE

NA 149. TEST.PD.USB4.EUSB.4 – DR_Swap after Entering USB4 Mode entry (Click to View Protocol Trace)

In VIF USB4_UFP_Supported field is NONE
In VIF USB4_DFP_Supported field is NONE

NA 150. TEST.PD.USB4.EUSB.5 – tEnterUSBWait check for USB4 DFP (Click to View Protocol Trace)

In VIF USB4_DFP_Supported field is NONE

NA 151. TEST.PD.USB4.CBL.1 – Enter_USB Message response of cable UUT-Valid Mode (Click to View Protocol Trace)

NA 152. TEST.PD.USB4.CBL.2 – Enter_USB Message response of Cable UUT-Invalid Mode (Click to View Protocol Trace)

153. Common Checks

PASS

Common_Check_PD_1_Check_Preamble - COMMON.CHECK.PD.1:

PASS

Check Preamble sequence and count - COMMON.CHECK.PD.1#1:

PASS

Common_Check_PD_2_Check_Message_Header -

PASS COMMON.CHECK.PD.2:

Check message header fields - COMMON.CHECK.PD.2#1:

PASS

Common_Check_PD_3_Check_GoodCRC - COMMON.CHECK.PD.3:

PASS

Check goodCRC response time - COMMON.CHECK.PD.3#1:

PASS

Check goodCRC message header fields - COMMON.CHECK.PD.3#2:

PASS

Common_Check_PD_4_Check_Atomic_Message_Sequence -

PASS COMMON.CHECK.PD.4:

Check Atomic message sequence - COMMON.CHECK.PD.4#1:

PASS

Common_Check_PD_5_Check_Unexpected_Messages_And_Signals -

PASS COMMON.CHECK.PD.5:

Unexpected Soft reset - COMMON.CHECK.PD.5#1:

PASS

Unexpected Hard Reset or a cable reset - COMMON.CHECK.PD.5#2:

PASS

Unexpected messages - COMMON.CHECK.PD.5#4:

PASS

Common_Check_PD_6_Control_Message - COMMON.CHECK.PD.6:

PASS

Number of data objects in header should be zero -
PASS COMMON.CHECK.PD.6#1:

Common_Check_PD_7_Source_Capability_Message -
PASS COMMON.CHECK.PD.7:

Check Source Capability message - COMMON.CHECK.PD.7#1:
PASS

Check Source Capability message - COMMON.CHECK.PD.7#2:
PASS

Check Data Objects field - COMMON.CHECK.PD.7#3:
PASS

Check First PDO - COMMON.CHECK.PD.7#4:
PASS

Check Fixed PDO - COMMON.CHECK.PD.7#5:
PASS

Check PPS Validation - COMMON.CHECK.PD.7#6:
PASS

Check Power Rules - COMMON.CHECK.PD.7#7:
PASS

Check PDO Consistency - COMMON.CHECK.PD.7#8:
PASS

Check PDO Sequence - COMMON.CHECK.PD.7#9:
PASS

Check Fixed PDO Voltage - COMMON.CHECK.PD.7#10:
PASS

Check Variable PDO Voltage - COMMON.CHECK.PD.7#11:
PASS

Check Battery PDO Voltage - COMMON.CHECK.PD.7#12:
PASS

Check AVS Validation - COMMON.CHECK.PD.7#13:
PASS

Common_Check_PD_8_Request_Message - COMMON.CHECK.PD.8:
PASS

Request messages fields check - COMMON.CHECK.PD.8#1:
PASS

Common_Check_PD_9_Structured_VDM - COMMON.CHECK.PD.9:
PASS

Structured VDM header field check - COMMON.CHECK.PD.9#1:
PASS

Common_Check_PD_10_Extended_Message_Header -
PASS COMMON.CHECK.PD.10:

Check Extended Message Header - COMMON.CHECK.PD.10#1:
PASS

Common_Check_PD_11_Source_Capability_Extended_Message -
PASS COMMON.CHECK.PD.11:

Source capabilities extended message fields check -
PASS COMMON.CHECK.PD.11#1:

Common_Check_PD_12_Check_Sink_Capabilities -
PASS COMMON.CHECK.PD.12:

Sink capabilities fields check - COMMON.CHECK.PD.12#1:
PASS

Common_Check_PD_13_Check_Correct_Use_of_Rp -
PASS COMMON.CHECK.PD.13:

No AMS sequence

No AMS sequence

Rp Level Validation - COMMON.CHECK.PD.13#1:
PASS

Common_Check_PD_14_Check_Hard_Reset - COMMON.CHECK.PD.14:
PASS

Check Hard_Reset basic timing - COMMON.CHECK.PD.14#1:
PASS

Common_Check_PD_15_Check_Sink_Capabilities_Extended_Message
PASS - COMMON.CHECK.PD.15:

Sink capabilities extended message fields check -
PASS COMMON.CHECK.PD.15#1:

COMMON_CHECK_PD3_1_Check_EPR_Request_Message -
PASS COMMON.CHECK.PD3.1:

EPR_Request messages fields check - COMMON.CHECK.PD3.1#1:
PASS

COMMON_CHECK_PD3_2_Check_EPR_Mode_Message -
PASS COMMON.CHECK.PD3.2:

EPR_Mode messages fields check - COMMON.CHECK.PD3.2#1:
PASS

COMMON_CHECK_PD3_3_Check_EPR_Source_Capabilities_Message -
PASS COMMON.CHECK.PD3.3:

VIF field EPR_Supported_As_Src check - COMMON.CHECK.PD3.3#1:
PASS

First Fixed PDO consistency check - COMMON.CHECK.PD3.3#2:
PASS

Fixed PDO check - COMMON.CHECK.PD3.3#3:
PASS

Programmable Power Supply APDO check -
PASS COMMON.CHECK.PD3.3#4:

EPR PDOs power rules check - COMMON.CHECK.PD3.3#5:
PASS

EPR PDOs consistency check - COMMON.CHECK.PD3.3#6:
PASS

Extended field check - COMMON.CHECK.PD3.3#8:
PASS

Data size extended header check - COMMON.CHECK.PD3.3#9:
PASS

SPR PDO check - COMMON.CHECK.PD3.3#10:
PASS

COMMON_CHECK_PD3_4_Check_EPR_Sink_Capabilities_Message -
PASS COMMON.CHECK.PD3.4:

EPR_Sink_Capabilities fields check - COMMON.CHECK.PD3.4#1:
PASS

154. Common Procedures
PASS

COMMON_PROC_PD_2_UUT_Sent_Get_Source_Cap -
PASS COMMON.PROC.PD.2:

Validate Get source capabilities message initiated by DUT -
PASS COMMON.PROC.PD.2#1:

DUT's Request message validation - COMMON.PROC.PD.2#2:
PASS

COMMON_PROC_PD_3_UUT_Sent_Get_Sink_Cap -
PASS COMMON.PROC.PD.3:

Validate Get sink cap message initiated by DUT -
PASS COMMON.PROC.PD.3#1:

COMMON_PROC_PD_4_UUT_Sent_Ping - COMMON.PROC.PD.4:
PASS

Ping message initiated by DUT - COMMON.PROC.PD.4#1:
PASS

COMMON_PROC_PD_5_UUT_Sent_PR_Swap - COMMON.PROC.PD.5:
PASS

PR_Swap valid condition check - COMMON.PROC.PD.5#1:
PASS

PR_Swap init and VIF field value comparison -
PASS COMMON.PROC.PD.5#2:

PR_Swap init and VIF field value comparison -
PASS COMMON.PROC.PD.5#3:

COMMON_PROC_PD_6_UUT_Sent_VCONN_Swap -
PASS COMMON.PROC.PD.6:

Vconn_Swap valid condition check - Tester Vconn Source -
PASS COMMON.PROC.PD.6#1:

Vconn_Swap init and VIF field value comparison -
PASS COMMON.PROC.PD.6#2:

tVCONNSourceOn Timer Validation - COMMON.PROC.PD.6#3:
PASS

Vconn_Swap valid condition check - DUT Vconn Source -
PASS COMMON.PROC.PD.6#4:

COMMON_PROC_PD_7_UUT_Sent_Discover_Identity_Request -
PASS COMMON.PROC.PD.7:

Validate Discover ID request message initiated by DUT -
PASS COMMON.PROC.PD.7#1:

Structured VDM Message Header check - COMMON.PROC.PD.7#2:
PASS

Tester's VDM response check - COMMON.PROC.PD.7#3:
PASS

COMMON_PROC_PD_8_UUT_Sent_Discover_SVIDs_Request -
PASS COMMON.PROC.PD.8:

Validate Discover ID request message initiated by DUT -
PASS COMMON.PROC.PD.8#1:

Structured VDM Message Header check - COMMON.PROC.PD.8#2:
PASS

Tester's VDM response check - COMMON.PROC.PD.8#3:
PASS

COMMON_PROC_PD_9_UUT_Sent_Attention - COMMON.PROC.PD.9:
PASS

Validate attention request message initiated by DUT -
PASS COMMON.PROC.PD.9#1:

Structured VDM message header check - COMMON.PROC.PD.9#2:
PASS

COMMON_PROC_PD_10_UUT_Sent_Request - COMMON.PROC.PD.10:
PASS

Validate request message initiated by DUT - COMMON.PROC.PD.10#1:
PASS

COMMON_PROC_PD_11_UUT_Sent_Source_Capabilities -
PASS COMMON.PROC.PD.11:

Validate Source capabilities message initiated by DUT -
PASS COMMON.PROC.PD.11#1:

DUT should respond with Accept - COMMON.PROC.PD.11#2:
PASS

DUT should send PS_RDY - COMMON.PROC.PD.11#3:
PASS

Wait Message - COMMON.PROC.PD.11#4:
PASS

COMMON_PROC_PD_12_UUT_Sent_DR_Swap -
PASS COMMON.PROC.PD.12:

Validate DR_Swap message initiated by DUT -
PASS COMMON.PROC.PD.12#1:

COMMON_PROC_PD_17_Tester_Sent_Vconn_swap_message -
PASS COMMON.PROC.PD.17:

VCONN present check - COMMON.PROC.PD.17#1:
PASS

PS_RDY is missing - COMMON.PROC.PD.17#2:
PASS

VCONN present check - COMMON.PROC.PD.17#3:
PASS

tVONNSourceOff timer check - COMMON.PROC.PD.17#4:
PASS

COMMON_PROC_PD3_1_Sink_Start_an_AMS - COMMON.PROC.PD3.1:
PASS

Sink Start AMS - COMMON.PROC.PD3.1#1:
PASS

COMMON_PROC_PD3_2_UUT_Sent_EPR_Source_Cap_message -
PASS COMMON.PROC.PD3.2:

Validate EPR_Source_Capabilities message initiated by UUT -
PASS COMMON.PROC.PD3.2#1:

UUT should respond with Accept - COMMON.PROC.PD3.2#2:
PASS

UUT should send PS_RDY - COMMON.PROC.PD3.2#3:
PASS

COMMON_PROC_PD3_3_UUT_Sent_EPR_Get_Source_Cap -
PASS COMMON.PROC.PD3.3:

Validate EPR Get Source Capabilities message initiated by DUT -
PASS COMMON.PROC.PD3.3#1:

DUT's EPR Request message validation - COMMON.PROC.PD3.3#2:
PASS

Requested Voltage and PDP - COMMON.PROC.PD3.3#3:
PASS

COMMON_PROC_PD3_4_UUT_Sent_EPR_Request -
PASS COMMON.PROC.PD3.4:

Validate EPR Request message initiated by DUT -
PASS COMMON.PROC.PD.3.4#1:

COMMON_PROC_PD3_5_Tester_Sent_EPR_Mode_Enter -
PASS COMMON.PROC.PD3.5:

Validate EPR Enter Enter fail initiated by DUT -
PASS COMMON.PROC.PD3.5#1:

VIF Field Has_Invariant_PDOs check - COMMON.PROC.PD3.5#2:
PASS

UUT Request message check - COMMON.PROC.PD3.5#3:
PASS

UUT sends a wait message - COMMON.PROC.PD3.5#4:
PASS

UUT sends PSRdy Message - COMMON.PROC.PD3.5#5:
PASS

VIF specified Source Capabilities - COMMON.PROC.PD3.5#6:
PASS

Source Cap message - COMMON.PROC.PD3.5#7:
PASS

UUT EPR_Mode Enter_Failed - COMMON.PROC.PD3.5#8:
PASS

UUT Not_Supported Message - COMMON.PROC.PD3.5#9:
PASS

UUT EPR_Mode Enter_Acknowledged - COMMON.PROC.PD3.5#10:
PASS

UUT VCONN_Swap Message - COMMON.PROC.PD3.5#11:
PASS

UUT EPR_Source_Capabilities Message - COMMON.PROC.PD3.5#12:
PASS

UUT EPR Contract - COMMON.PROC.PD3.5#13:
PASS

COMMON_PROC_PD3_6_UUT_Sent_EPR_Mode_Enter - COMMON.PROC.PD3.6:
PASS

Validate EPR_Mode_Enter initiated by DUT - COMMON.PROC.PD3.6#1:
PASS

Validate EPR_Mode_Enter response - COMMON.PROC.PD3.6#2:
PASS

Tester sends a Vconn_Swap message - COMMON.PROC.PD3.6#3:
PASS

Validate EPR_Mode Enter failed message - COMMON.PROC.PD3.6#4:
PASS

Validate SOP' Discover_Id and EPR Mode Enter Succeeded message - COMMON.PROC.PD3.6#5:
PASS

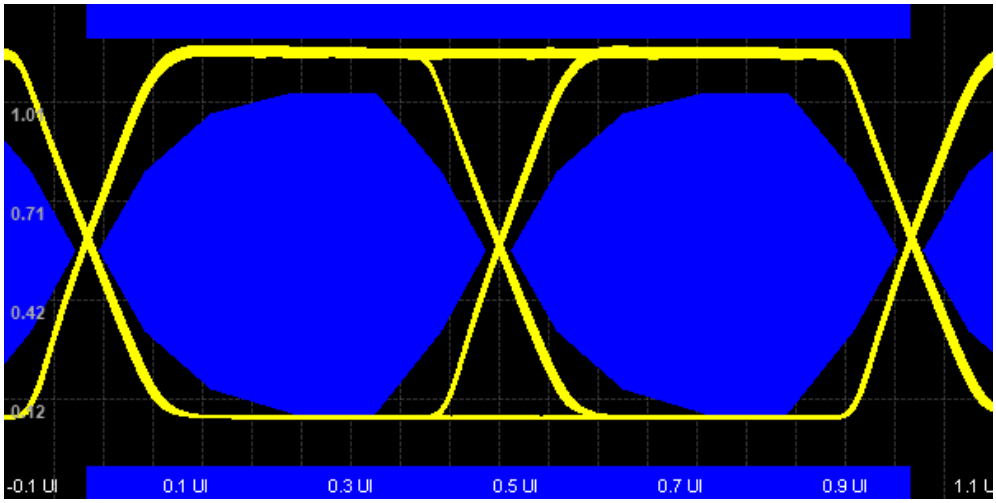
EPR_Source_Cap message - COMMON.PROC.PD3.6#6:
PASS

UUT establishes EPR contract - COMMON.PROC.PD3.6#7:
PASS

COMMON_PROC_PD3_7_Tester_Sends_EPR_KeepAlive_Message - COMMON.PROC.PD3.7:
PASS

Validate EPR_KeepAlive response message initiated by DUT - COMMON.PROC.PD3.7#1:
PASS

TEST.PD.PHY.ALL.2 - Eye diagram



DUT Information

Manufacturer	Shenzhen Huafurui Technology Co., Ltd.
Model Number	P90
Serial Number	1.1

Test Information

Test Lab	Shenzhen BCTC Testing Co., Ltd.
Test_Engineer	Willem Wang
Remarks	Remarks
Date_and_Time	2025/6/6 9:46:23

Controller and Instrument Information

Parameter	Value
GRL_USB_PD_Controller_Serial_No	GRL-C2-EPR-2024150
GRL_USB_PD_Software_Version	1.6.31.0
GRL_USB_PD_Firmware_Version	1.2.85
GRL USB-PD Ethernet Buffer Size	62K
GRL USB-PD Eload Firmware Version	1.5 / 1.5
GRL USB-PD PPS Firmware Version	4.0 / 4.0
Calibration	Calibration Success
RX mask Power selection	Neutral Power
Device_Type	DRP
Cable Type	GRL_SPL_EPR_CABLE_1
Impedance (milli ohm)	11
PD_Merged CTS Version	v.Q1-2025
USB_PD_Spec Version	Rev3.2 Ver1.1RC2
USB_Type_C_Spec Version	v2.3 Oct-2023
VIF_File_Name	Smart-Phone__P90__1.1__0.xml
Noise Pattern Generation:	Two-Tone Noise
Application mode	Informational
Disabled all Pop-up during test execution	False
Pop-up Timer	0
Rerun Enabled	False

Rerun Count	1
Rerun Iteration	0
UI Live Update	False
Execution Time(In Minutes)	41

Power Delivery 3.2 Tests Information

Parameter	Value
Connect EPR Test Fixture	False
FR_Swap AUTO Box Connected	False

Product Capabilities

Parameter	VendorInfoFile	GetCapabilities
VIF_Specification	3.32	
Vendor_Name	Smartphone	
Model_Part_Number	P90	
Product_Revision	1.1	
TID	0	
VIF_Product_Type	Port Product	
Certification_Type	End Product	
Port_Label	0	
Connector_Type	Type-C	
USB4_Supported	NO	
USB_PD_Support	YES	
PD_Port_Type	DRP	
Type_C_State_Machine	DRP	
Port_Battery_Powered	YES	
BC_1_2_Support	None	
Captive_Cable	NO	
PD_Spec_Revision_Major	3	
PD_Spec_Revision_Minor	1	
PD_Spec_Version_Major	1	
PD_Spec_Version_Minor	8	
PD_Specification_Revision	Revision 3	
SOP_Capable	YES	
SOP_P_Capable	NO	
SOP_PP_Capable	NO	
SOP_P_Debug_Capable	NO	
SOP_PP_Debug_Capable	NO	
Manufacturer_Info_Supported_Port	YES	
Manufacturer_Info_VID_Port	29CF	
Manufacturer_Info_PID_Port	5081	
Chunking_Implemented_SOP	YES	
Unchunked_Extended_Messages_Supported	NO	
Security_Msgs_Supported_SOP	NO	
Unconstrained_Power	NO	

Num_Fixed_Batteries	1	
Num_Swappable_Battery_Slots	0	
ID_Header_Connector_Type_SOP	USB Type-C Receptacle	
USB_Comms_Capable	YES	
DR_Swap_To_DFP_Supported	YES	
DR_Swap_To_UFP_Supported	YES	
VCONN_Swap_To_On_Supported	NO	
VCONN_Swap_To_Off_Supported	NO	
Responds_To_Discov_SOP_UFP	YES	
Responds_To_Discov_SOP_DFP	YES	
Attempts_Discov_SOP	YES	
Power_Interruption_Available	No Interruption Possible	
Data_Reset_Supported	NO	
Enter_USB_Supported	NO	
Type_C_Can_Act_As_Host	YES	
Type_C_Can_Act_As_Device	YES	
Type_C_Implements_Try_SRC	NO	
Type_C_Implements_Try_SNK	YES	
Type_C_Supports_Audio_Accessory	YES	
Type_C_Is_VCONN_Powered_Accessory	NO	
Type_C_Is_Debug_Target_SRC	YES	
Type_C_Is_Debug_Target_SNK	YES	
RP_Value	Default	
Type_C_Port_On_Hub	NO	
Type_C_Power_Source	Both	
Type_C_Sources_VCONN	NO	
Type_C_Is_Alt_Mode_Controller	NO	
Type_C_Is_Alt_Mode_Adapter	NO	
Product_Total_Source_Power_mW	5000	
Port_Source_Power_Type	Assured	
Host_Supports_USB_Data	YES	
Host_Speed	USB 2	
Host_Contains_Captive_Retimer	NO	
Host_Is_Embedded	YES	
Host_Suspend_Supported	NO	
Is_DFP_On_Hub	NO	
Device_Supports_USB_Data	1	
Device_Speed	USB 2	
Device_Max_USB2_Speed	High Speed	
Device_Contains_Captive_Retimer	NO	
EPR_Supported_As_Src	NO	
FR_Swap_Type_C_Current_Capability_As_Initial_Sink	FR_Swap not supported	
Master_Port	YES	
Has_Invariant_PDOs	YES	
Port_Managed_Guaranteed_Type	Guaranteed Capability	

EPR_Supported_As_Snk	NO	
Accepts_PR_Swap_As_Src	YES	
Accepts_PR_Swap_As_Snk	YES	
Requests_PR_Swap_As_Src	NO	
Requests_PR_Swap_As_Snk	NO	
FR_Swap_Supported_As_Initial_Sink	NO	
XID_SOP	0	
Data_Capable_As_USB_Host_SOP	YES	
Data_Capable_As_USB_Device_SOP	YES	
Product_Type_UFP_SOP	PDUSB Peripheral	
Product_Type_DFP_SOP	PDUSB Host	
DFP_VDO_Port_Number	0	
Modal_Operation_Supported_SOP	NO	
USB_VID_SOP	344F	
PID_SOP	0000	
bcdDevice_SOP	0000	
PD_Power_As_Source	5000	
USB_Suspend_May_Be_Cleared	YES	
Sends_Pings	NO	
Num_Src_PDOs	1 Src PDO	
PD_OC_Protection	NO	
PD_Power_As_Sink	18000	
No_USB_Suspend_May_Be_Set	YES	
GiveBack_May_Be_Set	NO	
Higher_Capability_Set	NO	
FR_Swap_Reqd_Type_C_Current_As_Initial_Source	FR_Swap not supported	
Num_Snk_PDOs	2 Snk PDOs	

Source Capabilities

Parameter	VendorInfoFile	GetCapabilities
Src_PDO_Supply_Type #1	Fixed	
Src_PDO_Peak_Current #1	100% IOC	
Src_PDO_Voltage #1	5000 mV	
Src_PDO_Max_Current #1	1000 mA	

Sink Capabilities

Parameter	VendorInfoFile	GetCapabilities
Snk_PDO_Supply_Type #1	Fixed	
Snk_PDO_Voltage #1	5000 mV	
Snk_PDO_Op_Current #1	2000 mA	
Snk_PDO_Supply_Type #2	Fixed	
Snk_PDO_Voltage #2	9000 mV	
Snk_PDO_Op_Current #2	2000 mA	

DUT Max Power

Power	NA